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# UPQC-S, A FRONTLINE DEPLOYABLE POWER LINE SOLUTION FOR HOLISTIC POWER QUALITY ENHANCEMENT

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**ABSTRACT**

The degradation of the electric power quality due to the escalated use of non-linear loads of commercial and domestic consumers of electric power connected via a distribution line, as well as those of industrial consumers of electric power connected via sub-transmission line, has necessitated to the invention of a variety of custom power devices. It seems more effective to insulate the power line from the effects of the non-linear loads and concurrently ensure a reliable, good quality power supply to all consumer loads, especially critical loads. The Unified Power Quality Conditioners (UPQC) is one such dedicated power quality improving device. Among the multitude of UPQC variants, in this paper the functioning of UPQC-S has been thoroughly investigated for diverse nonlinear loads operating under normal as well as abnormal loading conditions. UPQC-S has been designed and simulated for various nonlinear loading conditions under normal as well as abnormal network conditions. [side abnormalities.] The aforementioned simulation has been performed in MATLAB/SIMULINK.



## I. INTRODUCTION

Due to ever-increasing and accelerated usage of non-linear loads like domestic computing systems, LED lighting, LED Screen, compact fluorescent lamps, smartphone, power bank; inverter powered air conditioner, washing machine, microwave oven, induction heating system etc., the current and voltage harmonic magnitudes, in the power supply line have increased significantly [1],[2]. It is also to be noted that the power supply systems used in the above-mentioned equipment are compact in size, light weight, extremely efficient and provide good performance at the load end. These positive features are very desirable. But on the supply side, this has led to poor power supply quality, causing degraded performance of other AC supply powered equipment, heating of such equipment, increased transmission losses, line voltage fluctuations, insulation failures, interference issues in communication systems, etc.

It is to be noted that a lot of work has been done to make better the power quality along with reactive power compensation at sub-transmission level, by using various types of equipment ranging from LC Power Filters to FACTS based devices to STATCOM, SSSC, TSCS, TSC, UPFC, IPFC, etc. These FACTS based devices offer a satisfactory reactive power compensation but, an expensive and partially effective current/voltage harmonic compensation. One should keep in mind that the harmonics in the supply line, unbalanced voltage, voltage sag & swell, voltage flicker, etc., are a consequence of the non-linear loads connected at the distribution end.

To collectively address**,** all the above-mentioned power quality problems, power filters of passive type, active type as well as hybrid type have been used at the sub-transmission level. Passive filters have conventionally served to mitigate reactive power disturbances and harmonics, yet they suffer from several limitations such as bulky dimensions, resonance challenges, and susceptibility to the impedance characteristics of the power source, which can impact their effectiveness [3-5].

Generally, Parallel Active Power Filters (PAPFs) have been considered as current source employed in parallel to power line. But, the perception that PAPFs are ideal harmonic compensator is not correct, because the compensation characteristics of PAPF is influenced by the power line impedance (as with passive filters). PAPF is effective only for non-linear loads (such as phase-controlled thyristor rectifiers with large inductance for DC drives), which are a source of current harmonics. Non-linear loads like rectifiers with filter capacitor, which act as harmonic voltage source, cannot be compensated by PAPF.

However, the Series Active Power Filter (SAPF) are suitable for the Non-linear loads, which act as harmonic voltage source. Also, SAPF has the capability of providing compensation for voltage sag/swell, voltage flicker, source voltage imbalance. Thus, a combination of PAPF and SAPF, provide a complete and effective solution for enhancing power quality as a whole [6].

It is important to keep in mind that the origin of most power quality concerns is at the user end [1],[2], an integration of PAPF and SAPF connected at the distribution end would eliminate the entry of all causes which manifest in the power line as power quality issues. And, at the same time provide THD free supply voltage to all forms of load including critical loads. Shunt APFs (another name for PAPFs) as shunt current source, addresses current harmonic mitigation, reactive power compensation, and power factor betterment. On the other hand, Series APFs (SAPFs) as a series voltage source, targets voltage irregularities like sag/swell, voltage flicker, ensuring precise regulation of voltage at the load side [7]. PAPF operates as a static compensator (STATCOM) at the distribution end, and SAPF can function as a load voltage regulator (VR) at the distribution end. Hence, PAPF as DSTATCOM and SAPF as DVR can be integrated into one power quality enhancing device at the distribution end [8-10]. Such an integrated power device, has been given the name of UPQC in the literature, an abbreviation for Unified Power Quality Conditioner [3-5],[10]. A plethora of classifications and structural arrangements of UPQC are found in the literature [4],[11], but the focus of this paper is the right shunt type of UPQC-S [12], in which DSTATCOM and DVR are connected back-to-back as Voltage Source Converter, across a common DC bus capacitor. In UPQC-S, the DSTATCOM fully takes care of all current harmonic compensation, injects reactive power partially and absorbs active power from the power line. Whereas, the DVR infuses a voltage in series between the PCC and the load end at a predefined phase angle and DVR injects both active power and reactive power into the power line. The miniscule real power absorbed by the DSTATCOM, accounts for the switching losses and for maintaining the voltage of the common DC bus Capacitor connected across the VSCs of DSTATCOM & DVR [4],[13]. Overall, this arrangement elevates power quality, by managing both real and reactive power requirements. The power circuit of UPQC is discussed in section II. The general design flow of UPQC-S is discussed in section III. The control approach for UPQC-S is described in section IV. The MATLAB-SIMULINK based performance response of UPQC-S for various nonlinear loads under normal and abnormal network side conditions is discussed in section V. The conclusion of the paper is in section VI.

## II. CIRCUIT CONFIGURATION OF UPQC

All UPQC configurations have back-to-back connected shunt and series converters to a DC Bus Capacitor or a battery [4]. The Series converter is popularly identified as Dynamic Voltage Restorer (DVR) and Shunt converter as DSTATCOM. Both DVR and DSTATCOM are generally chosen to be topologically, Voltage Source Inverters. DSTATCOM compensates the current harmonics, reactive power and DVR compensates for voltage sag/swell problems in AC distribution system. The Block diagram of UPQC incorporated with power system is as depicted in Figure 1.

Based on the location of connection, UPQC is classified either as right-side shunt UPQC or left-side shunt UPQC. Right-side shunt UPQC, wherein the DVR is connected adjacent to the PCC and DSTATCOM is connected adjacent to the load. Left-side shunt UPQC, wherein the DVR is connected adjacent to the load and DSTATCOM is connected adjacent to the PCC. Right-side shunt UPQC is preferred over Left-side shunt UPQC, as the right-side shunt configuration, results in a simpler control strategy and a lower VA rating of both DSTATCOM and DVR [5]. UPQC is further classified as UPQC-Q, UPQC-P and UPQC-S [4]. Take note that this classification is purely based on the voltage compensation approach used, with no change in the power circuit of the UPQC, as depicted in Figure 2.

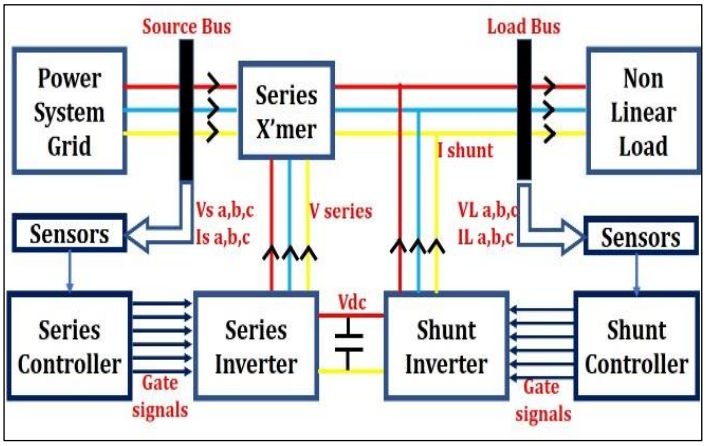


Figure 1: Block diagram of UPQC-S with power system.
Source: Authors, (2024).

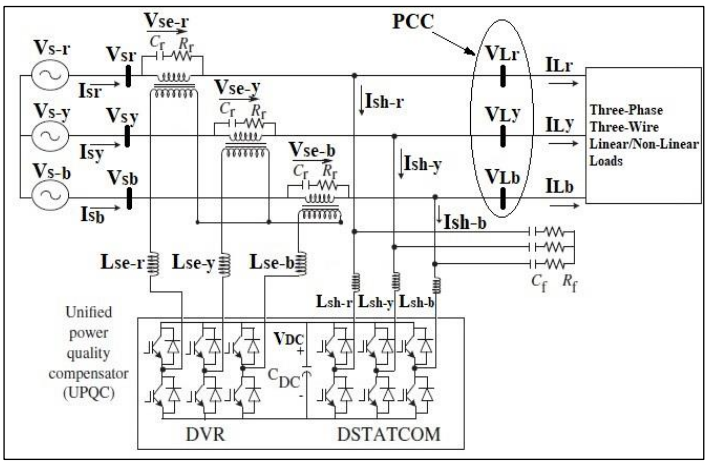


Figure 2: Connection diagram of electrical power grid with UPQC-S for non linear load.
Source: Authors, (2024).

It is in the context of this compensation approach, that the Table 1. has been worked out, as below. Table 1 differentiates between the three of them, for various compensating actions and energy storage requirement of a common capacitor or battery energy storage system. In the right-side shunt UPQC-S, both VSCs have equal reactive power rating, which is half of the reactive power of the load. Also, real power rating is same for both VSCs, due to their to a common DC bus capacitor.

In UPQC-S, if one of the connections VSCs absorbs real power from the power line, the other VSC must be injecting an equal amount of real power, into the supply line [11]. The circuit connections for UPQC-S are as shown in Figure 2. It is in the context of this compensation approach, that the Table 1. has been worked out, as below. Table 1 differentiates between the three of them, for various compensating actions and energy storage requirement of a common capacitor or battery energy storage system. In the right-side shunt UPQC-S, both VSCs have equal reactive power rating, which is half of the reactive power of the

load. Also, real power rating is same for both VSCs, due to their connection to a common DC bus capacitor.

Table 1: Selection criterions of UPQC.

| **Compensation Operation** | **UPQC-Q** | **UPQC-P** | **UPQC-S** |
|---|---|---|---|
| DVR injected voltage angle w.r.t source current | Orthogonal | In phase | 0ºto360º |
| DVR Injects/Absorbs Reactive Power (Q) | Yes | No | Yes |
| DVR Injects/Absorbs Active Power (P) | No | Yes | Yes |
| DVR Provides Voltage Sag Compensation | Yes | Yes | Yes |
| DVR Provides Voltage Swell Compensation | No | Yes | Yes |
| DC link support via Capacitor | Yes | No | Yes |
| DC link support via battery | No | Yes | Yes |
| DSTATCOM Injects/Absorbs Reactive Power (Q) | Yes | Yes | Yes |
| DSTATCOM Injects/Absorbs Active Power (P) | Yes | No | Yes |

Source: Authors, (2024).

In UPQC-S, if one of the VSCs absorbs real power from the power line, the other VSC must be injecting an equal amount of real power, into the supply line [11]. The circuit connections for UPQC-S are as shown in Figure 2.

The phasor diagram to visualize the compensating actions by DVR and DSTATCOM, in case of voltage Sag, in UPQC-S, as reflected in Figure 3 [14]. The series voltage $V_{SE}$ is infused at $\Psi_{SE}$ angle relative to sagging source voltage $V'_t$ by DVR. This voltage compensation causes a change in the current compensation ($I_{SH}$ *to* $I'_{SH}$) provided by DSTATCOM. In this case, DVR and DSTATCOM, both inject reactive power, but DVR injects active power, whereas DSTATCOM absorbs active power.

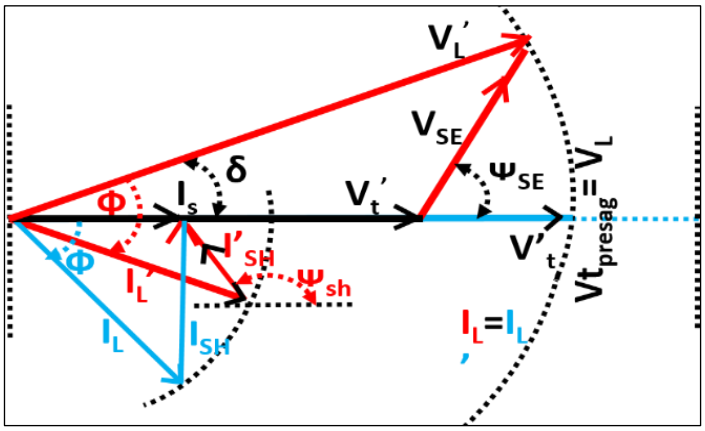


Figure 3: Phasor diagram for voltage sag in UPQC-S.
Source: Authors, (2024).

In Figure 4, series $V_{SE}$ is infused at $\Psi_{SE}$ angle w.r.t. to swelling source voltage $V'_t$ by DVR. This voltage compensation causes a change in the current compensation ($I_{SH}$ *to* $I'_{SH}$) provided by DSTATCOM. In this case, DVR and DSTATCOM, both inject reactive power, but DVR absorbs active power and DSTATCOM injects active power.

It is through this absorption of the active power (either by DVR or DSTATCOM) under the supply voltage sag or swell, that the voltage of the common DC link capacitor is maintained [4], [13].

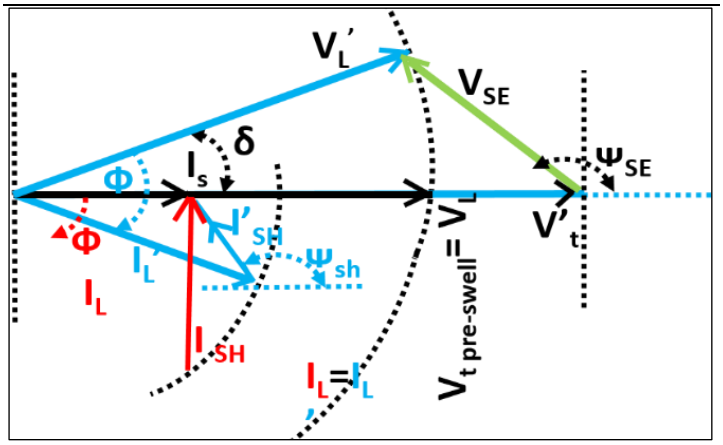


Figure 4: Phasor diagram for voltage swell compensation in UPQC-S.
Source: Authors, (2024).

## III. INSIGHT OF DESIGNING OF UPQC-S

The Design of UPQC-S, is broadly, the calculation of the Volt-Ampere rating of DSTATCOM, DVR and DVR Injection Transformer. This calculation is based on multiple predefined parameters related to supply, load and designer specific choices.

The supply side parameters are supply voltage, supply frequency, supply impedance, % supply voltage sag/swell. The load side parameters are load active power, load power factor. The designer choices are about the overloading factor, allowable variation in capacitor voltage, allowable time for DC link capacitor voltage recovery etc. Using the above-described parameters, the below design flow can be used to calculate the Volt Amp rating of DSTATCOM, DVR and Injection Transformer, Voltage & current rating of semiconductor switch used in the VSCs of DSTATCOM and DVR, the value of capacitance of common DC link as well as the magnitude of its voltage, the inductance and the current rating of AC inductors used in DSTATCOM and DVR and the associated ripple filters. The steps and the equations involved in designing has been depicted in the flow chart shown in Figure 5.

## IV. CONTROL STRATEGY OF UPQC-S

From a multitude of control strategies in the time domain [15], along with the controller design procedure [16], fixed frequency PWM controllers, a combination of PWM and Hysteresis controller to Space Vector PWM Controllers [17-19], that can be applied for the comprehensive current and voltage compensation, a much simpler hysteresis band-based control approach has been used [20]. This control approach is applied for power quality compensation in a 3P3W, supply system at distribution end [19]. Here the synchronous reference frame (SRF) theory, has been applied for controlling DSTATCOM and PQ (Active-Reactive Power) theory, has been applied for controlling DVR. The objective of the control strategy for the DSTATCOM, is ($I_{SH}$) compensation, during supply voltage sag/swell [21],[22] and to maintain the set voltage of the DC Bus capacitor, by absorbing real power, from the power line. Figure 6 & Figure 7 represent control strategies for the same to achieve complete harmonic as well as reactive current. The objective of the control strategy for the DVR, is to preserve the rated load voltage during

voltage sag/swell [21],[22] by infusing voltage in series with supply voltage at a pre-calculated angle ($\Psi_{SE}$) to the supply voltage, approach used for DSTATCOM and DVR, is as reflected in Figure 6 and Figure 7 respectively.

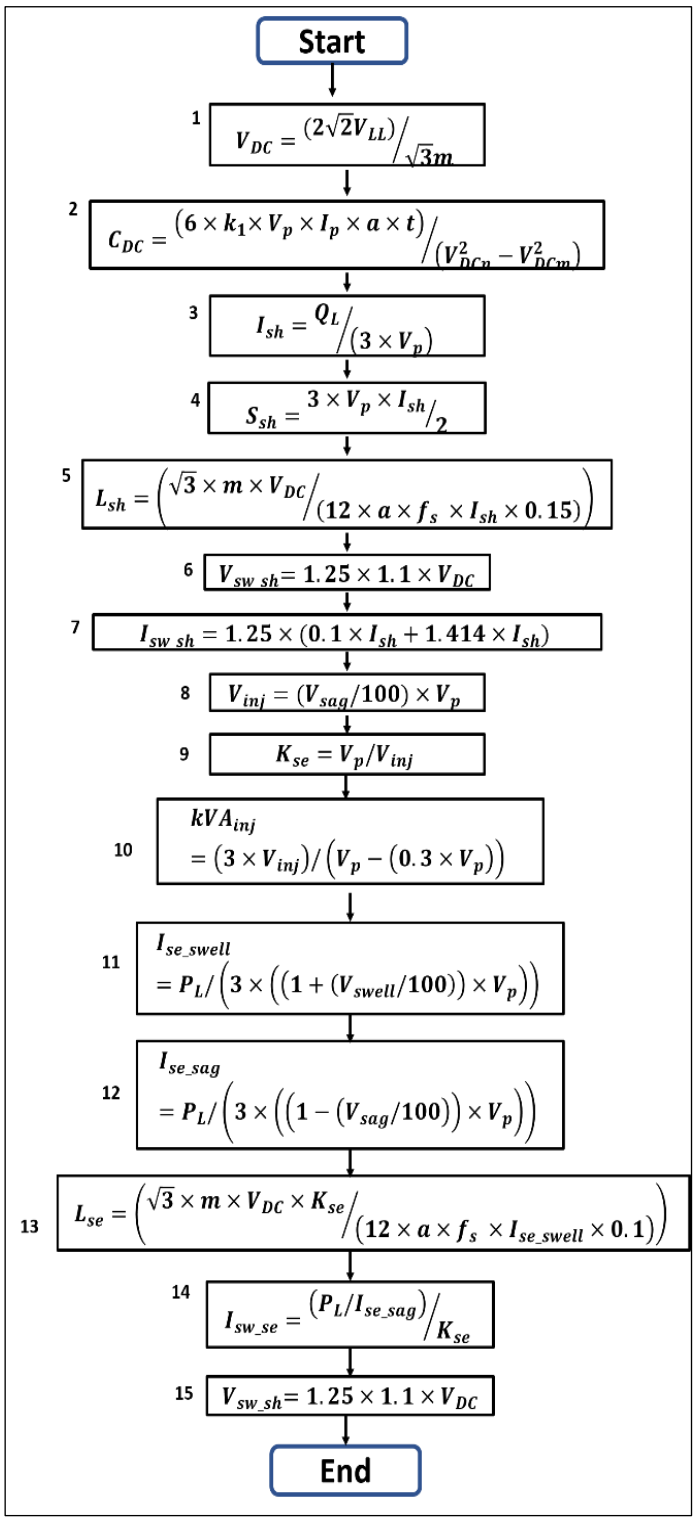


Figure 5: UPQC-S Design Flow chart.
Source: Authors, (2024).

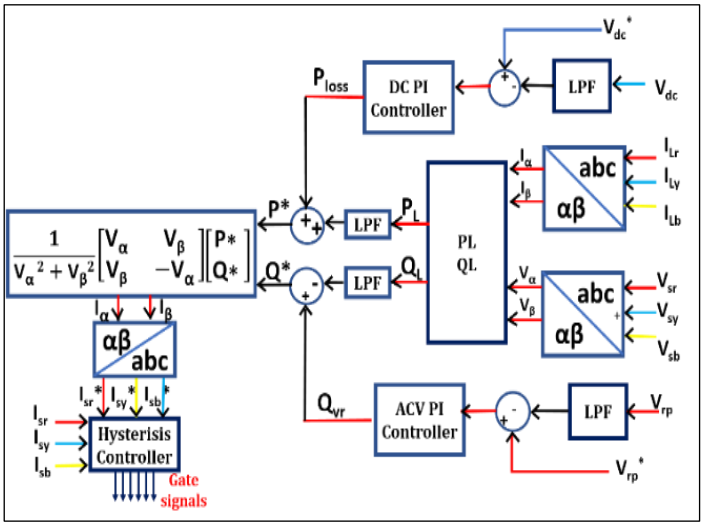


Figure 6: Control approach for DSTATCOM.
Source: Authors, (2024).

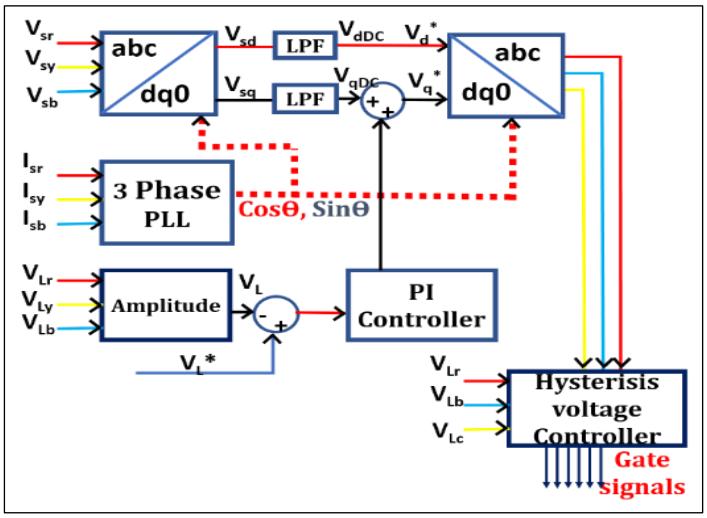


Figure 7: Control approach for DVR.
Source: Authors, (2024).

The control approach is to be tested for not only for achieving near unity power factor on the supply side, but also for load balancing and cancelling voltage & current harmonics, requiring the DVR to inject/absorb real and reactive power, but without discharging the preset DC bus capacitor voltage. The control as well as the load voltage regulation under supply voltage sag/swell, flicker, notch conditions, specifically in a 3P3W distribution system for linear and non-linear loads.

## V. MATLAB SIMULINK IMPLEMENTATION

### V.1 SIMULATION MODEL

The Figure 8 reflects implementation of UPQC-S in MATLAB-SIMULINK. Extensive simulation tests are conducted to assess the efficacy of a 3P3W UPQC in addressing various power quality issues such as voltage/current harmonics, voltage sags/swells, voltage distortion, voltage supply imbalance, voltage flicker, voltage notches, load current unbalance, and reactive power compensation. Figure 9 and Figure 10 show the SIMULINK implementation of SRF theory and PQ theory respectively.

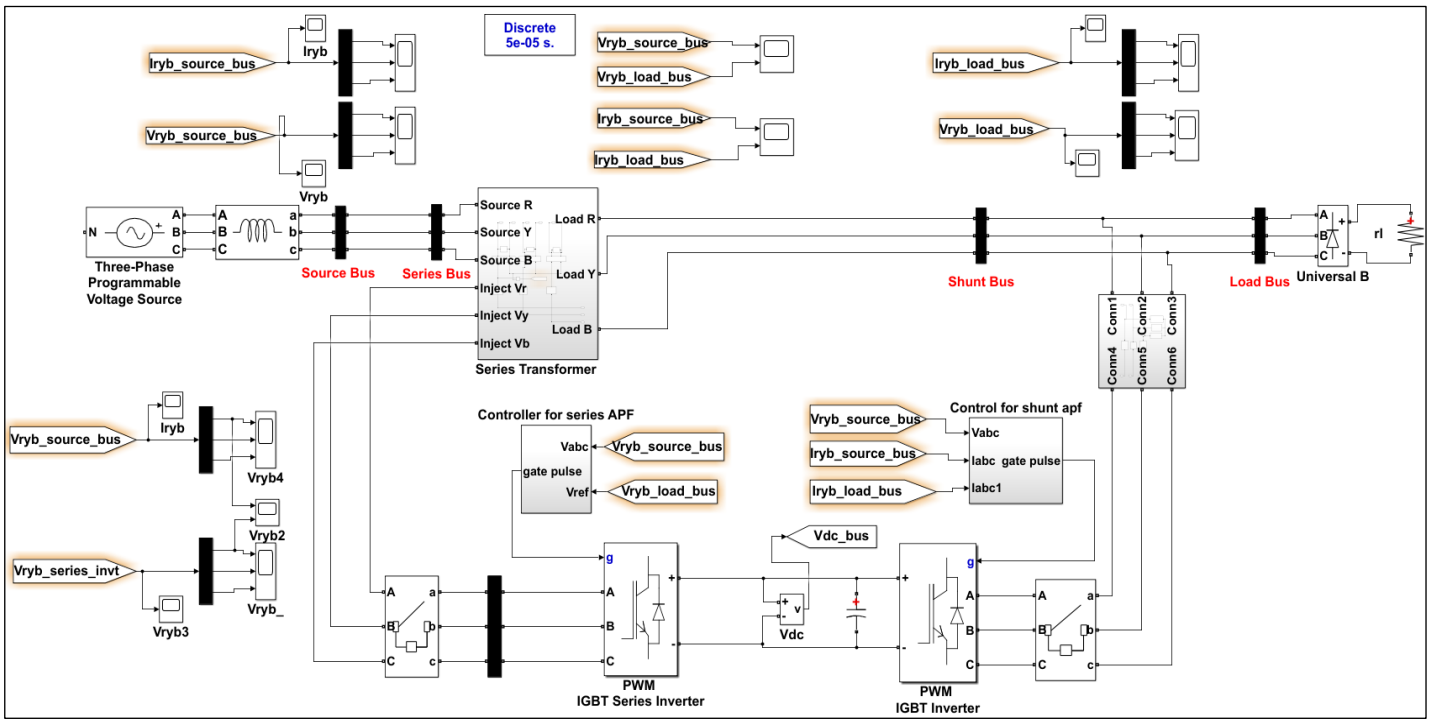


Figure 8: Matlab Simulink implementation of UPQC-S system.
Source: Authors, (2024).

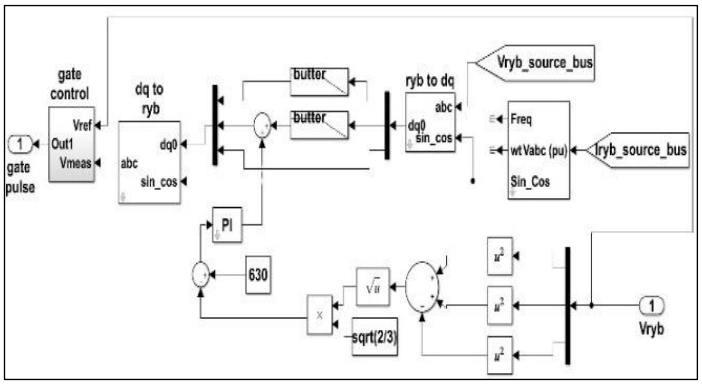


Figure 9: Series Inverter Controller (DVR).
Source: Authors, (2024).

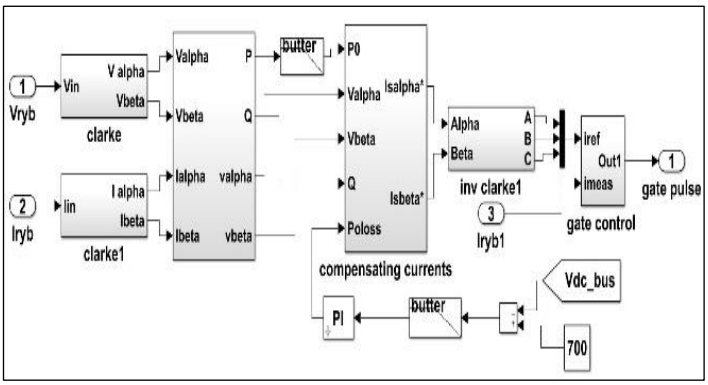


Figure 10: Shunt inverter controller (DSTATCOM).
. Source: Authors, (2024).

## V.2 SIMULATION SET POINTS

The load configurations include a 3-Φ rectifier with RL/RC load, a 3-Φ thyristor bridge rectifier with RL load, a 3-Φ unbalanced resistive load, and a 3-Φ induction motor. The setpoint values of parameters for load is given in Table 2. Table 3. outlines the parameters of the UPQC system, with the source voltage specified as (3 Phase, 415V, 50 Hz).

Table 2: Simulink model Load set point values.

| Sr. | Parameters | Set Point |
|---|---|---|
| **1.** | Load: Non Linear Load (3P 3W) | $R_L$ = 30 ohm, L=1.0 mH (Series) |
| **2.** | Load: Non Linear Load with controlled rectifier (3P 3W) | $R_L$ = 30 ohm, L=1.0 mH, α=$20^0$ (Series) |
| **3.** | Load: Non Linear Load (3P 3W) | $R_L$=10 ohm, C=1000 microF (Parallel) |
| **4.** | Load: Rating of Asynchronous Squirrel cage machine | P= 7460 VA, V=415 V, F=50 Hz |
| **5.** | Load: Non Linear Load (3P 3W) | $R_L$ = 30 ohm, L=1.0 mH (Series) |

Source: Authors, (2024).

Table 3: Simulink model UPQC set point values.

| Sr. | Parameters | Set Point |
|---|---|---|
| **1.** | DC Bus voltage ($V_{dc}$), | 700V |
| **2.** | DC Bus Capacitor ($C_{dc}$) | 6000 µF |
| **3.** | DSTATCOM: AC Inductor for phase leg of VSC ($L_{sh}$) | 6 mH |
| **4.** | DSTATCOM: Ripple Filter | $R_f$=5Ω, $C_f$=5 µF |
| **5.** | DSTATCOM: KVA Rating | 13 kVA |
| **6.** | DSTATCOM: Max. Current | 32 A |
| **7.** | DVR: Injection Transformer | 415/75,12.8kVA |
| **8.** | DVR: Interfacing Inductor | $L_{se}$=10mH |
| **9.** | DVR: Ripple Filter | $R_f$=5Ω, $C_f$=5 µF |
| **10.** | DVR: KVA Rating | 13 kVA |
| **11.** | DVR: Maximum Current | 32 A |

Source: Authors, (2024).

### V.3 SIMULATION RESULTS

Various operating scenarios of UPQC-S are considered, and depicted in different cases, and discussed in this section.

#### V.3.1 CASE 1A: UPQC-S CORRECTIVE RESPONSE FOR UCNLL.

In this scenario, an uncontrolled bridge rectifier with an RL load is employed to evaluate the behaviour of UPQC-S. Its voltage corrective response under non-linear load conditions is depicted in Figure 11. Upon activation of UPQC-S at 0.1 seconds (DVR activation following DSTATCOM activation), it is found that supply and load voltages are minimally affected by Uncontrolled Non-Linear Load (UCNLL). Consequently, the series voltages ($V_{se}^{ryb}$) remain close to sinusoidal. Figure 12 illustrates the current profile for the corrective response by UPQC-S. It shows the compensating shunt currents Fig.12 (b), which cancel out current harmonics generated by uncontrolled rectifier. Notably, after 0.1 second, the source current approaches sinusoidal behaviour. Figure 13 and Figure 14 depict THD for voltage before and after employing UPQC-S, which are 1.15% and 0.18%, respectively.

Furthermore, current THD, depicted in Figure 15 and Figure 16, is reduced from 30.15% to:

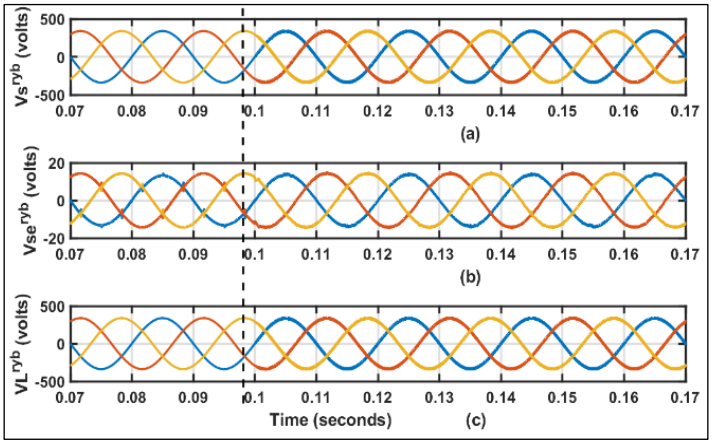


Figure 11: Voltage profile of UPQC-S corrective response for UCNLL.
Source: Authors, (2024).

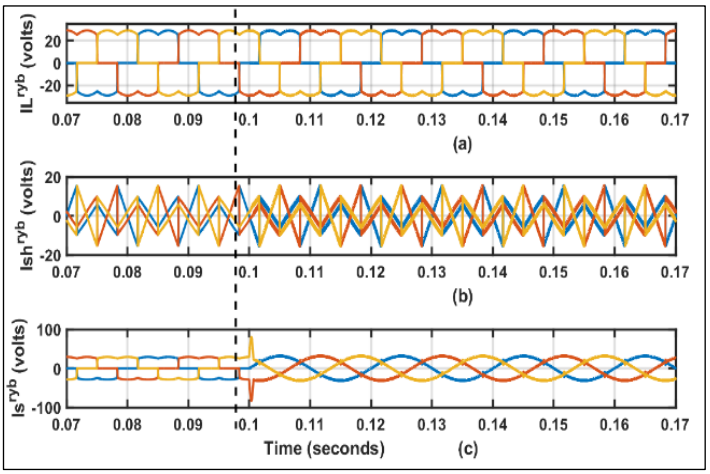


Figure 12: Current profile of UPQC-S.
Source: Authors, (2024).

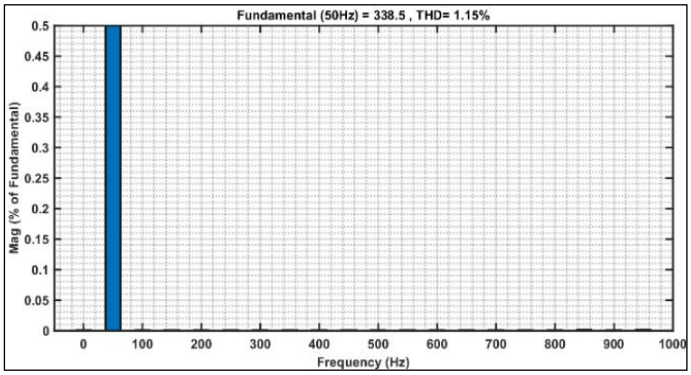


Figure 13: Voltage THD before UPQC-S corrective response for UCNLL.
Source: Authors, (2024).

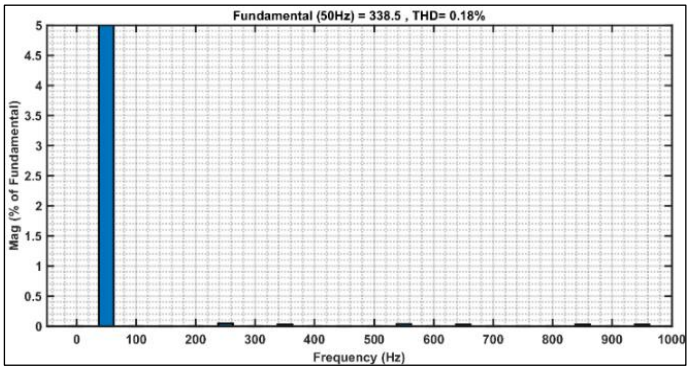


Figure 14: Voltage THD after UPQC-S corrective response for UCNLL.
Source: Authors, (2024).

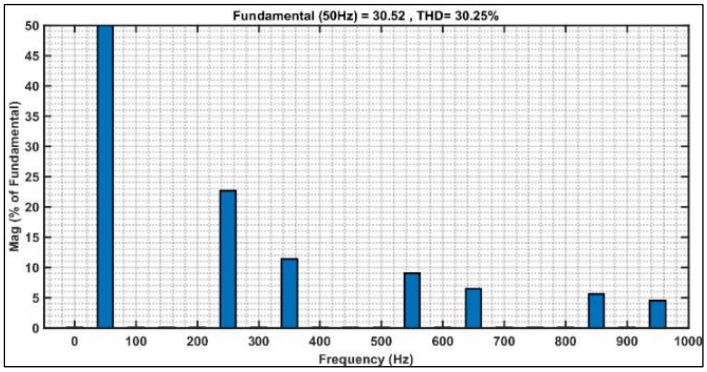


Figure 15: Current THD before UPQC-S corrective response for UCNLL.
Source: Authors, (2024).

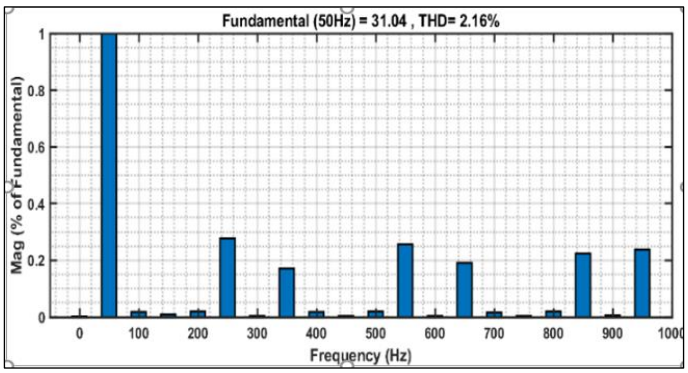


Figure 16: Current THD after UPQC-S corrective response for UCNLL.
Source: Authors, (2024).

### V.3.2 CASE 1B: UPQC-S CORRECTIVE RESPONSE FOR CNLL

In Case-1B, a controlled bridge rectifier with an RL load is utilized to assess the performance of UPQC-S. The Controlled Non-Linear Load (CNLL) operates with a firing angle of 20°. As depicted in Figure 17, the voltage correction response of UPQC-S under non-linear load conditions is illustrated. At 0.1 seconds, UPQC-S is activated (DVR following DSTATCOM), revealing spikes in both source and load voltages during CNLL operation as shown in Figure 17. Consequently, DVR injects voltage ($V_{se}^{ryb}$) to mitigate these spikes and all voltage harmonics generated by switching operations.

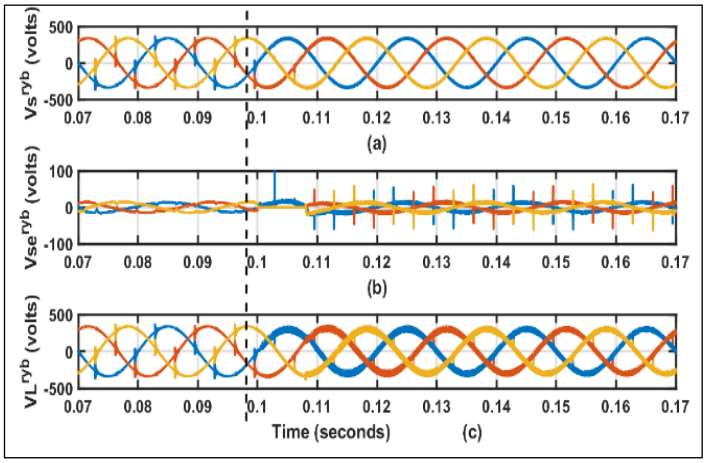


Figure 17: Voltage profile of UPQC-S corrective response for CNLL.
Source: Authors, (2024).

Figure 18 reflects the current profile for the corrective response by UPQC-S, indicating that it generates shunt currents ($I_{sh}^{ryb}$), which are injected into the system to cancel out current harmonics generated by the CNLL. Notably, after 0.1 seconds, the source current approaches sinusoidal behavior. Figure19 and Figure 20 display the voltage THD before and after employing UPQC-S, which are 5.31% and 0.82%, respectively. Moreover, current THD improves from 32.90% to 3.34%, complying with the limits outlined in the IEEE-519 standard, which is reflected in Figure 21 & Figure 22.

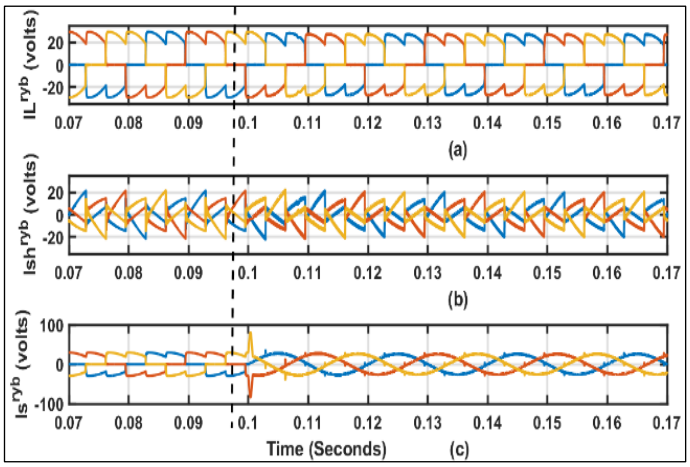


Figure 18: Current profile of UPQC-S corrective response for CNLL.
Source: Authors, (2024).

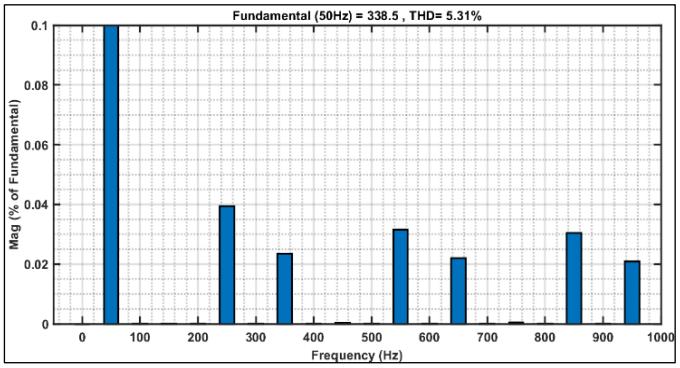


Figure 19**:** Voltage THD before UPQC-S corrective response for CNLL.
Source: Authors, (2024).

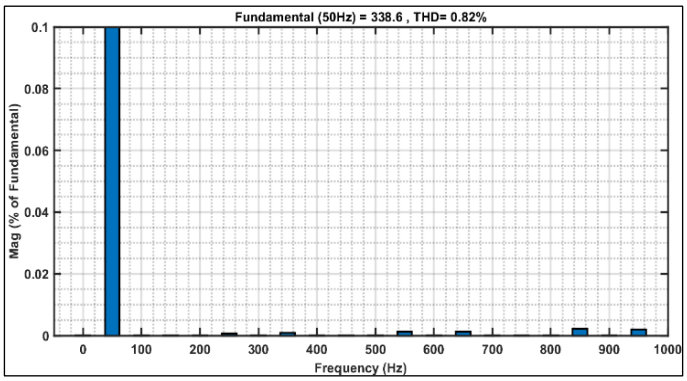


Figure 20: Voltage THD after UPQC-S corrective response for CNLL.
Source: Authors, (2024).

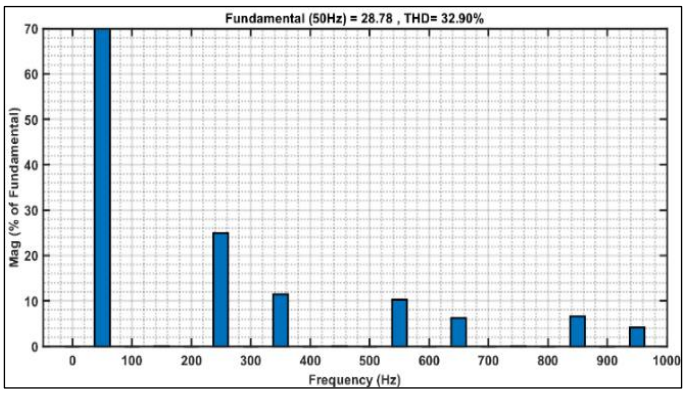


Figure 21: Current THD before UPQC-S corrective response for CNLL.
Source: Authors, (2024).

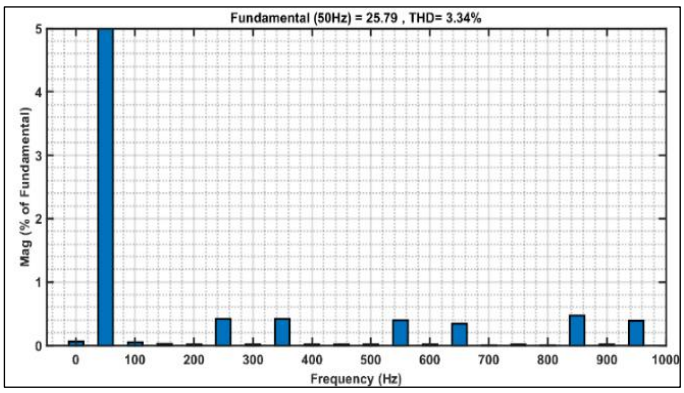


Figure 22: Current THD after UPQC-S corrective response for CNLL.
Source: Authors, (2024).

### V.3.3 CASE 2: UPQC-S CORRECTIVE RESPONSE FOR CAPACITIVE LOAD

In this Case, an uncontrolled rectifier with RC load is employed to evaluate performance of UPQC-S.Fig.23 illustrates the current correction response of UPQC-S under non-linear conditions with an RC load. At 0.6 seconds, UPQC-S is activated (DVR following DSTATCOM), resulting in an improvement in the distorted source current, which gradually approaches near sinusoidal behaviour, as depicted in Figure 23(a).

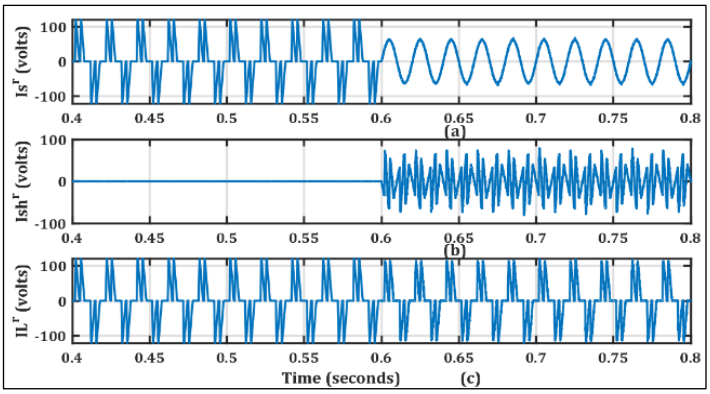


Figure 23: Current profile of UPQC-S corrective response for capacitive load.
Source: Authors, (2024).

Figure 23(b) and Figure 23(c) depicts the shunt ($I_{sh}^{r}$) and load ($I_{L}^{r}$) currents respectively. It is notable that the capacitive type load injects a significant amount of current harmonics into the source, as evident from Figure 24, which shows a current THD of 81.06%. However, after 0.6 seconds, the source current approaches sinusoidal behaviour due to shunt compensating current ($I_{sh}^{r}$) injection. Figure 25 present the current THD after the insertion of UPQC-S, which is reduced to 3.62%, complying with the limits specified in the IEEE-519 standard.

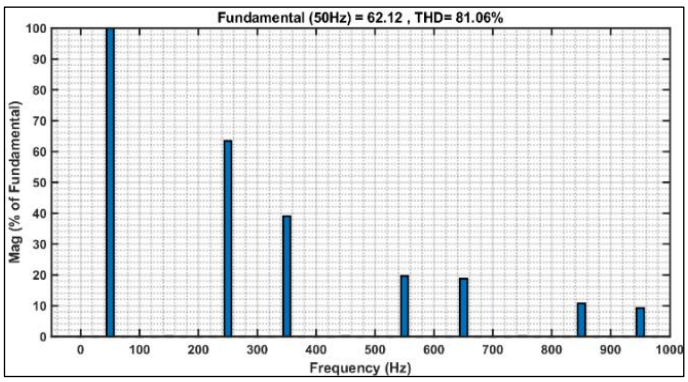


Figure 24: Current THD before UPQC-S corrective response for capacitive load.
Source: Authors, (2024).

### V.3.4 CASE 3: UPQC-S CORRECTIVE RESPONSE FOR UNBALANCE VOLTAGE SUPPLY.

In Case 4 scenario, an unbalanced voltage (0.2pu) is deliberately introduced from the source side, spanning from 1.4 s to 1.7 s and from 1.9 s to 2.2 s, while considering a non-linear load. During this period, the magnitude of the R phase is increased from 1.4 s to 1.7 s.

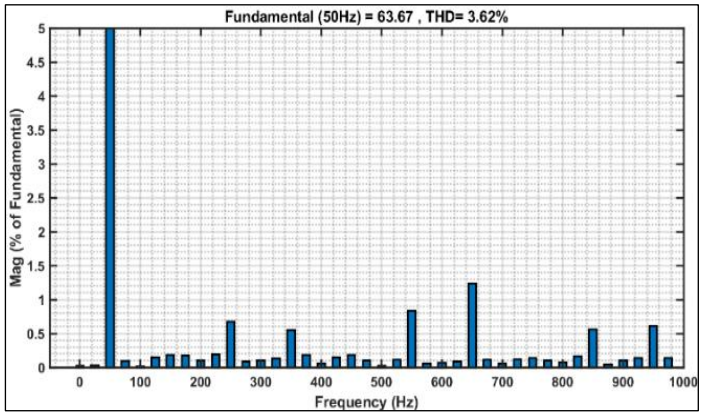


Figure 25: Current THD after UPQC-S corrective response for capacitive load
Source: Authors, (2024).

and then decreased from 1.9 s to 2.2 s, as evidenced in Figure 26 (a), (b) & (c). DVR intervenes by injecting series voltage in a manner that effectively compensates for the unbalance, ensuring that the load voltage remains constant throughout this unbalanced condition. The corrective response of UPQC-S is depicted in Figure 27 and Figure 28, which respectively show the voltage THD and current THD during the unbalanced supply condition.

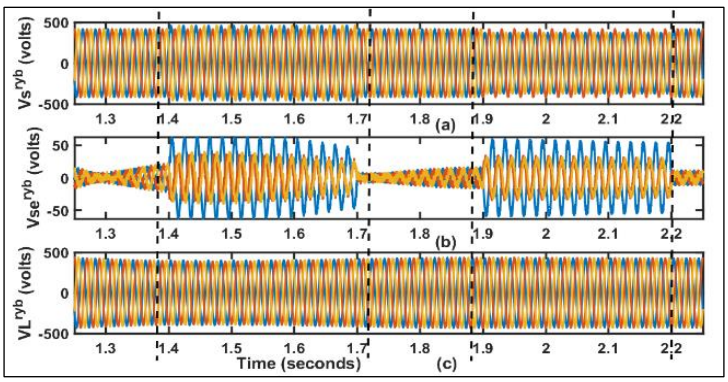


Figure 26: Voltage profile of UPQC-S corrective response for unbalance voltage supply.
Source: Authors, (2024).

### V.3.5 CASE 4A: UPQC-S CORRECTIVE RESPONSE DURING VOLTAGES SAG.

The dynamic behavior of the UPQC-S for a non-linear load condition is shown in Figure 29 (a), (b) & (c). It reflects transient response of the UPQC-S, during a voltage sag scenario, specifically when a non-linear load is connected. At 0.1 sec, voltage sag of 0.3 pu, in the source voltage ($V_{s}^{r}$) occurs for 10 cycles, during which it is found that load voltage ($V_{L}^{r}$) in Figure 29 (c) is effectively regulated to a constant amplitude both during the voltage sag and under normal operating conditions. Notably, it is during the sag period that the DVR injects voltage ($V_{se}^{r}$) to preserve the load voltage, as illustrated in Figure 29(b). Furthermore, both voltage and current THD remain within the limits outlined by the IEEE-519 standard, as demonstrated in Figure 30 and Figure 31, respectively.

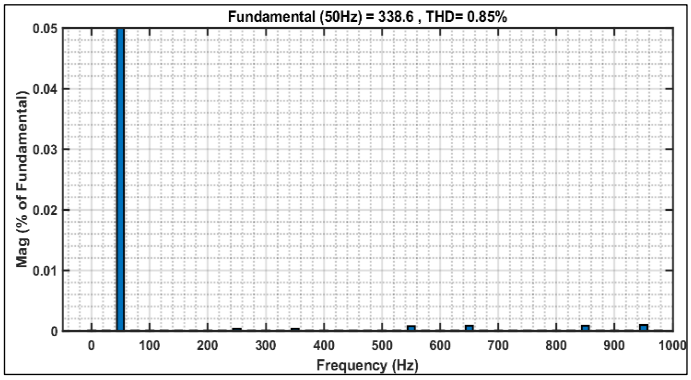


Figure 27**:** Voltage THD, after Corrective response for unbalance voltage supply.
Source: Authors, (2024).

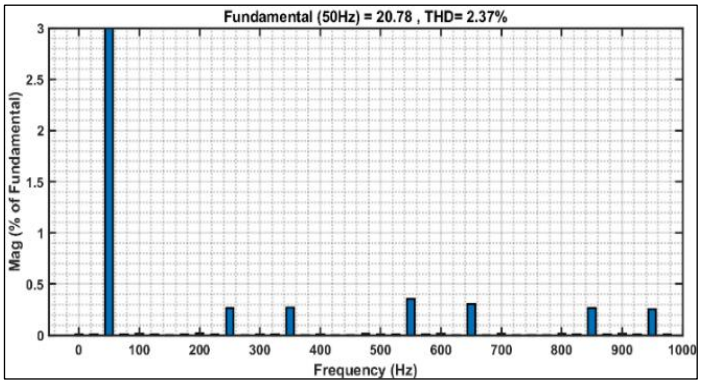


Figure 28: Current THD, after corrective response for unbalance voltage supply.
Source: Authors, (2024).

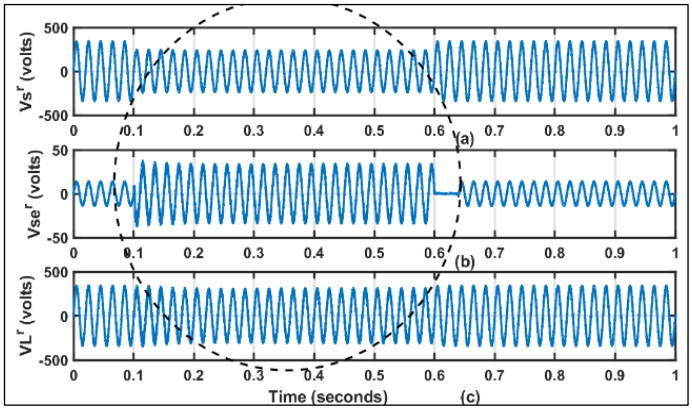


Figure 29: Voltage Profile of UPQC-S corrective response during voltages sag.
Source: Authors, (2024).

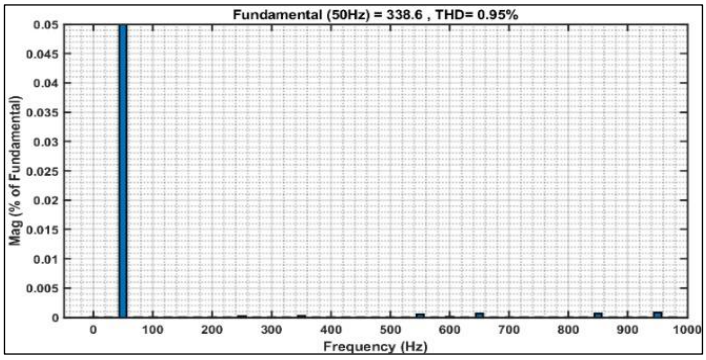


Figure 30: Voltage THD, after UPQC-S corrective response during voltages sag.
Source: Authors, (2024).

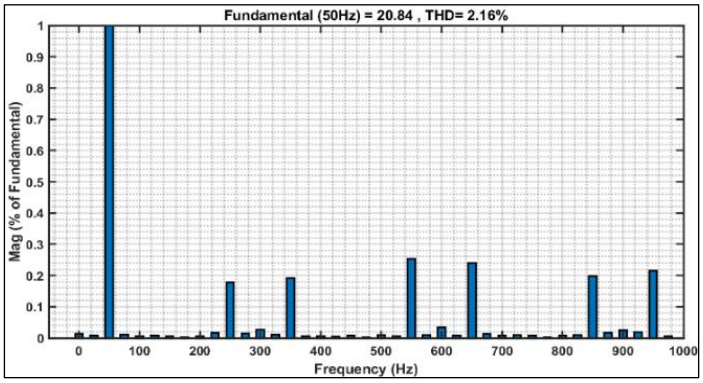


Figure 31: Current THD, after UPQC-S corrective response during voltages sag.
Source: Authors, (2024).

### V.3.6 CASE 4B: UPQC-S CORRECTIVE RESPONSE DURING VOLTAGES SWELL.

Figure 32 depicts the transient response of the UPQC-S, during voltage swell scenario, for a non-linear load. At the 0.1 sec, a voltage swell in the source voltage of 0.3 pu occurs for 10 cycles. Interestingly, it is found that the load voltage ($V_L^r$) in Figure 32 (c), remains regulated to a constant amplitude both during the voltage swell and under normal condition. Notably, only during the swell event, DVR infuses voltage ($V_{se}^r$) to preserve the load voltage.

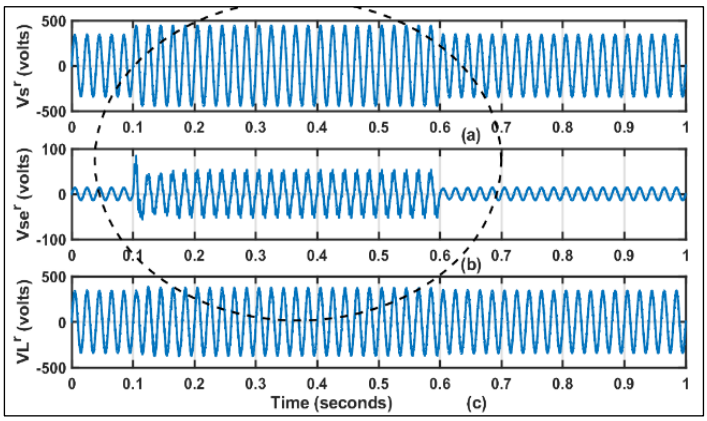


Figure 32: Voltage profile of UPQC-S corrective response during voltages swell.
Source: Authors, (2024).

Furthermore, both voltage and current THD remain within the limits outlined by the IEEE-519 standard, as demonstrated in Figure 33 and Figure 34, respectively.

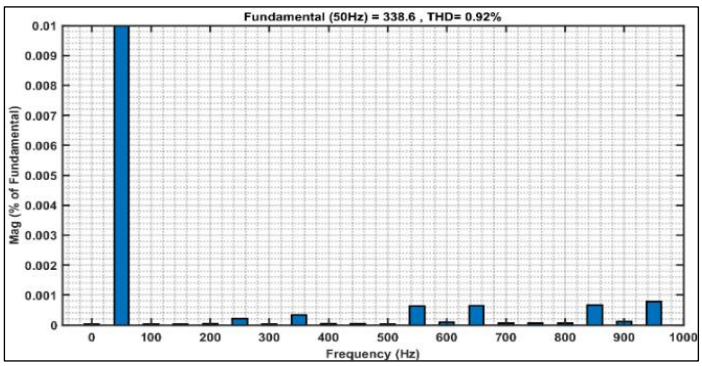


Figure 33: Voltage THD, after UPQC-S corrective response during voltages swell.
Source: Authors, (2024).

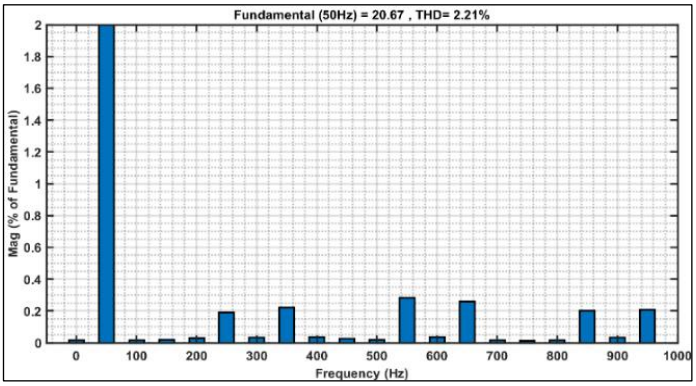


Figure 34: Current THD after UPQC-S corrective response during voltages swell.
Source: Authors, (2024).

### V.3.7 CASE 5: UPQC-S COMPENSATIVE RESPONSE FOR INDUCTION MOTOR LOAD.

In this scenario, the nonlinear load is an induction motor. UPQC-S is activated at 0.6s. Prior to activation, the compensating current ($I_{sh}^{ryb}$) as reflected in Figure 35 is negligible, also the reactive power($Q_s$) drawn from the source is considerably high as shown in Figure 36 (a). Following activation at 0.6s, the load reactive power requirement from supply reduces significantly from 3927 VAR to 698 VAR. This required reactive power for the induction motor is then supplied by DSTATCOM ($Q_{sh}$) , as demonstrated in Figure 36 (c).

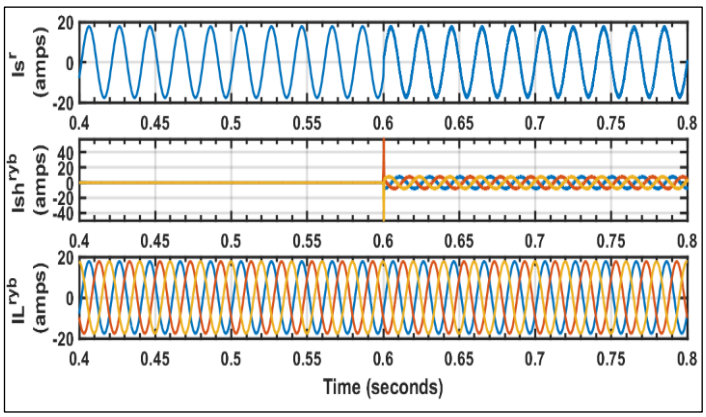


Figure 35**:** Current profile of UPQC-S compensative response for induction motor load.
Source: Authors, (2024).

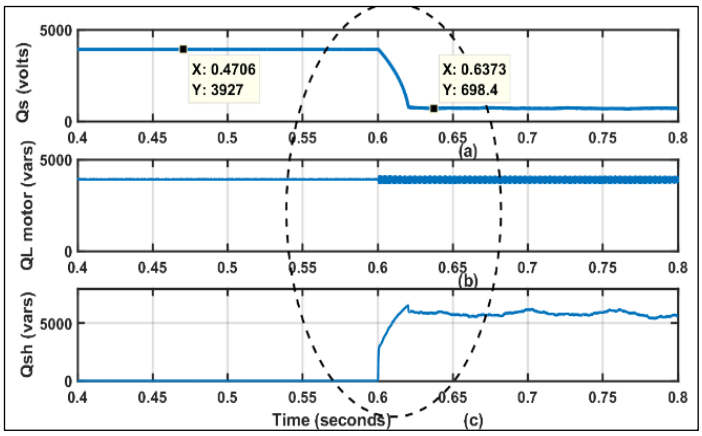


Figure 36: Reactive power profile of UPQC-S compensative response for Induction Motor load.
Source: Authors, (2024).

### V.3.8 CASE 6: UPQC-S CORRECTIVE RESPONSE DURING VOLTAGE FLICKER.

In this case, voltage fluctuations occur intermittently at the source side, specifically between time intervals of 0.1s to 0.13s and 0.2s to 0.23s.The performance evaluation of UPQC-S is conducted under these conditions. Figure 37 illustrates the DVR intervention by injecting series voltage ($V_{se}^{ryb}$) to preserve the load voltage ($V_L^{ryb}$) ,from being affected by fluctuations.

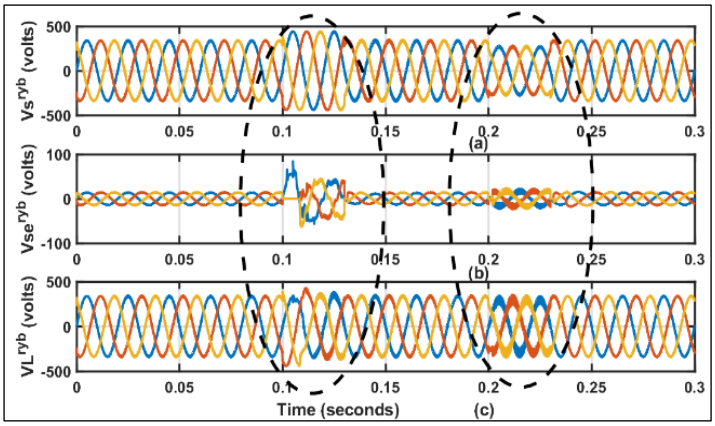


Figure 37**:** Voltage profile of UPQC-S corrective response during voltage flicker.
Source: Authors, (2024).

### V.3.9 CASE 7: UPQC-S CORRECTIVE RESPONSE DURING HARMONIC INJECTION

In this case, at the onset of 0.1s, distortion in the source voltage is intentionally induced across all three phases by introducing specific harmonics-namely the 5$^{th}$ harmonic (set at 15% of the source voltage) and the 7$^{th}$ harmonic (set at 20% of the source voltage). It is illustrated in Fig.38, that DVR, promptly initiates the process of harmonic compensation by injecting a combined signal comprising the 5$^{th}$ and 7$^{th}$ harmonics. This intervention effectively leads to the generation of a voltage waveform free from distortions, ensuring optimal conditions for nonlinear loads.

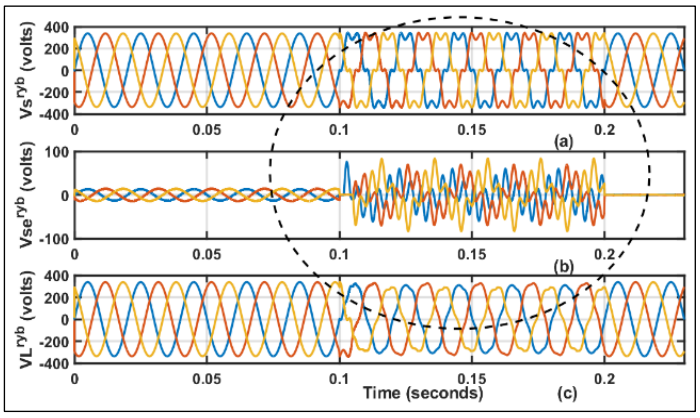


Figure 38: Voltage profile of UPQC-S corrective response during harmonic injection.
Source: Authors, (2024).

It is depicted in Figure 39 and Figure 40, voltage THD has been significantly brought down from 20.43% to 1.92%. It can be seen from Figure 41, that the capability of mitigating imbalance in

source current caused by imbalance in load current has been satisfactorily achieved. Distinct differences in load phase currents are used for identifying any irregularities in load distribution. Typically, load imbalances are observed due to the utilization of a three-phase

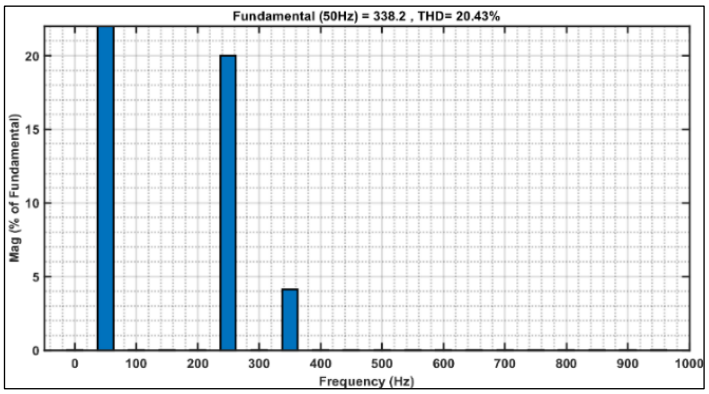


Figure 39: THD of source voltage during harmonic injection.
Source: Authors, (2024).

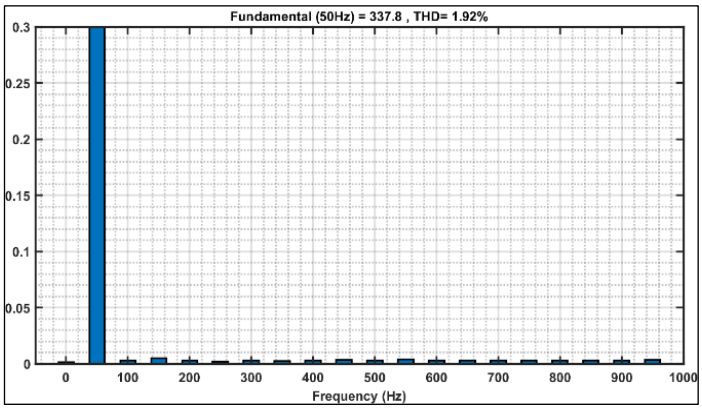


Figure 40: THD of load voltage during harmonic injection.
Source: Authors, (2024).

### V.3.10 CASE 8: LOAD IMBALANCE

Unbalanced linear load. Specifically, load resistors of 20Ω, 40Ω, and 60Ω are employed for phase-r, phase-y, and phase-b, respectively. Upon activation of the UPQC-S at 0.1s, as depicted in Figure 41, the source current ($I_s^{ryb}$) achieves equilibrium, with compensating shunt currents ($I_{sh}^{ryb}$).

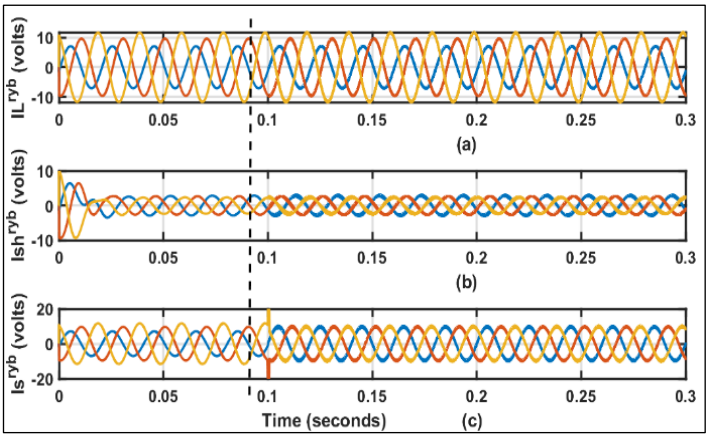


Figure 41: Corrective response of UPQC-S during load imbalance.
Source: Authors, (2024).

## VI CONCLUSIONS

This paper advocates, a simple and generalized, design procedure of UPQC-S. A conceptual analysis of UPQC-S for all the power quality related issues, has been carried out via MATLAB/SIMULINK. The major key points of the aforementioned simulation are as follows:

1. The DVR section of the proposed UPQC-S under the hysteresis band controller is capable of compensating for source voltage sag/swell, source voltage imbalance, source voltage flicker and notches.
2. Source current remains within the THD limits set in IEEE-519 for all type of controlled and uncontrolled non-linear load, by using UPQC-S. Further, for RC-type load (Capacitor filter based Resistive Loads), the source current THD is substantially alleviated to 3.62% from 81.06%.
3. The DVR and DSTATCOM work in synchronism to obtain the load-reactive power compensation/Load imbalance, for linear as well non-linear load.

Table 4: ABBREVIATIONS.

| | |
|---|---|
| UPQC-S | Unified Power Quality Conditioner -Apparent power (S) |
| UCNLL | Uncontrolled Non-Linear Load |
| CNLL | Controlled Non-Linear Load |
| THD | Total Harmonic Distortion |
| PAPF | Parallel Active Power Filter |
| SAPF | Series Active Power Filter |
| DVR | Dynamic Voltage Restorer |
| DSTATCOM | Distributed Static Synchronous Compensator |
| PCC | Point of Common Coupling |
| IPFC | Inter Liner Power Flow Controller |
| SSSC | Static Synchronous Series Compensator |
| TSCS | Thyristor Switched Controlled Capacitor. |
| TSC | Thyristor Switched Capacitor. |
| UPFC | Unified Power Flow Control |
| STATCOM | Static Synchronous Compensator |

Source: Authors, (2024).

## VII CONFLICT OF INTEREST

"The authors declare that there are no conflicts of interest or any financial interest regarding the publication of this manuscript".

## VIII AUTHOR CONTRIBUTION STATEMENT

**Conceptualization:** Sajid M. Patel, Mohammedirfan I Siddiqui and Dhaval R. Patel.
**Methodology:** Sajid M. Patel, Mohammedirfan I Siddiqui and Dhaval R. Patel.
**Investigation:** Sajid M. Patel, Mohammedirfan I Siddiqui and Dhaval R. Patel.
**Discussion of results:** Sajid M. Patel, Mohammedirfan I Siddiqui and Dhaval R. Patel.
**Writing – Original Draft:** Sajid M. Patel, Mohammedirfan I Siddiqui and Dhaval R. Patel.
**Writing – Review and Editing:** Sajid M. Patel, Mohammedirfan I Siddiqui and Dhaval R. Patel.
**Resources:** Sajid M. Patel, Mohammedirfan I Siddiqui and Dhaval R. Patel.
**Pictures & Images:** Sajid M. Patel, Mohammedirfan I Siddiqui and Dhaval R. Patel.
**Supervision:** Sajid M. Patel, Mohammedirfan I Siddiqui and Dhaval R. Patel.

**Approval of the final text:** Sajid M. Patel, Mohammedirfan I Siddiqui and Dhaval R. Patel.

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