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RESEARCH ARTICLE OPEN ACCESS

IMPACT OF GRAIN BOUNDARIES ON THE ELECTRICAL CHARACTERISTICS AND BREAKDOWN BEHAVIOR OF POLYCRYSTALLINE SILICON PIN DIODES: A SIMULATION STUDY

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ABSTRACT

In this paper, we present a comprehensive two-dimensional simulation program designed to model the intricate electrical characteristics of reverse-biased lateral polysilicon PIN diodes. Our methodology involves the numerical resolution of a system of partial differential equations, specifically Poisson's equation and the continuity equations for both electrons and holes, incorporating the significant effects of impact ionization. By employing this simulation approach, we are able to accurately derive the current-voltage (I-V) characteristics of the reverse-biased structure, including detailed analyses of breakdown phenomena. The geometrical model employed in our study assumes that the polysilicon layer is composed of a sequence of crystallites with well-defined mean grain sizes. These crystallites are separated by lateral grain boundaries that run parallel to the metallurgical junction, influencing the overall electrical behavior of the diode. Our simulation results provide critical insights into the impact of these grain boundaries on the diode's performance, highlighting the role of trapping centers and their effect on the electric field distribution and carrier dynamics within the device. Furthermore, this study discusses the implications of our findings for the design and optimization of polysilicon-based electronic components, suggesting potential improvements in device fabrication and performance. The comprehensive analysis presented in this paper not only enhances the understanding of polysilicon PIN diodes but also contributes to the broader field of semiconductor device engineering.

I. INTRODUCTION

Polycrystalline silicon, commonly referred to as polysilicon or PC-Si, has become an integral material in the integrated circuit industry due to its versatile electrical properties [1-3], which can vary significantly. This material's application spans various electronic components, including thin-film transistors (TFTs), photovoltaic cells, PN junction diodes, and both PIN and Schottky diodes [4-6]. Polysilicon is composed of numerous small silicon crystals, known as crystallites, which are typically about a tenth of a micron in size and exhibit the same crystalline structure as single-crystal silicon [7], [8].

The unique structure of polycrystalline silicon can be attributed to its composition of monocrystalline grains of different orientations [9], [10]. These grains are separated by highly disordered, narrow regions known as grain boundaries, which are typically only a few angstroms wide and are rich in defects [11-13]. These grain boundaries play a crucial role in determining the

electrical properties of polysilicon [14], [15]. The deep energy states within these boundaries can trap free carriers, significantly influencing the material's conductivity and behavior in electronic devices [16-18].

The significance of polysilicon in semiconductor technology was first highlighted by Seto in 1975 [19], who proposed a one-dimensional analytical model to describe the electrical properties of polycrystalline silicon films [20]. This model underscored the impact of grain boundaries on the material's electrical characteristics [21], particularly in terms of carrier trapping and mobility reduction [22-24]. Subsequent research has expanded on Seto's foundational work, exploring the complex interactions between crystallites and grain boundaries, and their implications for device performance.

As polysilicon continues to be a material of choice in the fabrication of advanced electronic components, understanding its properties and behavior under various conditions remains critical. This paper focuses on a two-dimensional simulation study of the electric characteristics of reverse-biased lateral polysilicon PIN diodes. By numerically solving the system of partial differential equations, including Poisson's equation and the continuity equations for both electrons and holes, we aim to elucidate the current-voltage (I-V) characteristics of these diodes, particularly considering the effects of impact ionization and breakdown phenomena.

This study's insights are expected to contribute significantly to the design and optimization of polysilicon-based electronic components, enhancing their performance and reliability in various applications.

II. PHYSICAL MODEL

The physical model that provides the IV characteristics is typically based on solving a system of differential equations. Solar cells, like all semiconductor devices, are modelled using five basic equations: Poisson's equation, the continuity equations for both electrons and holes, and the two transport equations, which are collectively described by the drift-diffusion model [25].

$$\begin{cases} \frac{\partial^2\varphi}{\partial x}+\frac{\partial^2\varphi}{\partial y}=\frac{q}{\varepsilon}(-p+n-\Sigma p_T+\Sigma n_T-N_D^+ +N_A^-) \\ -\frac{1}{q}\left(\frac{\partial^2 j_h}{\partial x}+\frac{\partial^2 j_h}{\partial y}\right)=r_h-g_h \\ \frac{1}{q}\left(\frac{\partial^2 j_e}{\partial x}+\frac{\partial^2 j_e}{\partial y}\right)=r_e-g_e \\ j_{nx}=-q\,n\,\mu_n\frac{\partial\varphi}{\partial x}+q\,D_n\frac{\partial n}{\partial x} \\ j_{ny}=-q\,n\,\mu_n\frac{\partial\varphi}{\partial y}+q\,D_n\frac{\partial n}{\partial y} \end{cases} \quad (1)$$

The advantage of this model is that it accounts for the effects of trapping centers, which significantly influence the behavior of semiconductor devices [26]. To solve these equations, the discretization method employed is the finite difference method, and the Scharfetter-Gummell approximation is used to enhance the accuracy of the numerical solution [27].

III. NUMERICAL SOLUTION

Solving the system of equations that describe the behavior of a semiconductor device is challenging due to the large number of unknown variables. To make the problem more manageable, we simplify it to a system with three unknowns: the electrostatic potential (φ), and the electron (n) and hole (p) concentrations. These equations are highly nonlinear because of the exponential terms present in the expressions for n and p.

Among the numerical methods available for solving differential equations, we employ the finite difference method. In this approach, after discretizing the study domain, we replace the differential equations with difference equations. This process transforms the continuous problem into a discrete one that can be solved using numerical techniques.

To solve the resulting system, we use the algorithm developed by Gummel [28]. This algorithm iteratively solves the three equations of the system by updating each unknown in turn. Each equation is solved based on estimated values for the other two unknowns. After solving one equation, the corrected value of the unknown is used in the subsequent equations. This iterative process is repeated until the solutions for all three equations converge, ensuring an accurate and stable solution for the system.

This method's iterative nature allows for handling the nonlinearities in the equations effectively, providing a robust framework for analyzing the IV characteristics of semiconductor devices.

IV. GEOMETRIC AND PHYSICAL MODEL A PIN DIODE BASED ON POLYCRYSTALLINE SILICON

The geometric and physical model of the PIN diode based on polycrystalline silicon is fundamental to understanding its electrical characteristics. The PIN diode structure consists of three distinct zones along the X axis: the P+ region, the intrinsic (I) region, and the N region. The dimensions of these regions are detailed in Table 1 below.

Table 1: Dimensions of the PIN Diode.

Zone	Dimension
P+	100
I	200-800 nm
N	700 nm
First joint grain (Lg1)	100 nm
Crystallite size (Lg)	160 nm

Source: Authors, (2024).

The geometric model assumes that the polysilicon layer comprises a series of crystallites with defined mean grain sizes. These crystallites are separated by lateral grain boundaries, which are parallel to the metallurgical junction (see Figure .1).

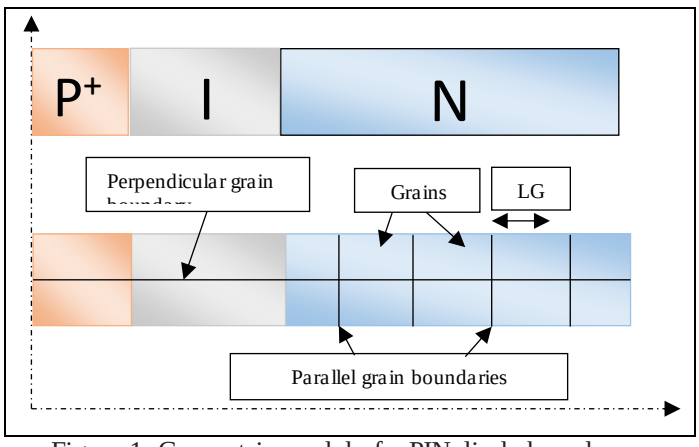

Figure 1: Geometric model of a PIN diode based on polycrystalline silicon.
Source: Authors, (2024).

In this model, the grain boundaries play a significant role in the electrical properties of the diode. These boundaries are populated with traps, both acceptor and donor types, with a surface density denoted as NTA and NTD, respectively. These traps are assumed to be monoenergetic and are located exclusively within the grain boundaries, which are set at a thickness of 1 nm. The traps

can be amorphous, with energy levels ETA and ETD positioned symmetrically in the middle of the bandgap.

The ionization rate of these states follows the classical Shockley-Read-Hall (SRH) formalism, which is critical for understanding the recombination and generation processes within the diode. The SRH model describes the ionization rates for donor-type and acceptor-type traps as follows:

For the discrete density of states of ionized donor-type traps:

$$N_{TD}^{+} = N_{TD}\frac{C_P \cdot p + C_n \cdot N_C \exp\left(\frac{E_{TD}-E_C}{kT}\right)}{C_n\left(n+N_C\exp\left(\frac{E_{TD}-E_C}{kT}\right)\right)+C_P\left(p+N_V\exp\left(\frac{E_V-E_{TD}}{kT}\right)\right)} \quad (2)$$

$$N_{TA}^{-} = N_{TA}\frac{C_n \cdot n + C_p N_V \exp\left(\frac{E_V-E_{TA}}{kT}\right)}{C_n\left(n+N_C\exp\left(\frac{E_{TA}-E_C}{kT}\right)\right)+C_P\left(p+N_V\exp\left(\frac{E_V-E_{TA}}{kT}\right)\right)} \quad (3)$$

Where:

N+TD: the density of states discrete traps ionized donor-type.

N-TA: the density of states discrete traps ionized acceptor –type.

Cn and CP are the coefficients of capture and emission of electrons and holes and NTA, NTD, respectively, the total density of states discrete donor and acceptor traps located at ETA and ETD.

The traps at the grain boundaries significantly influence the electrostatic potential and carrier concentrations within the diode, affecting the overall device performance, particularly under reverse bias conditions. Understanding these interactions is essential for optimizing the design and functionality of polycrystalline silicon PIN diodes.

V. ENERGY BAND STRUCTURES

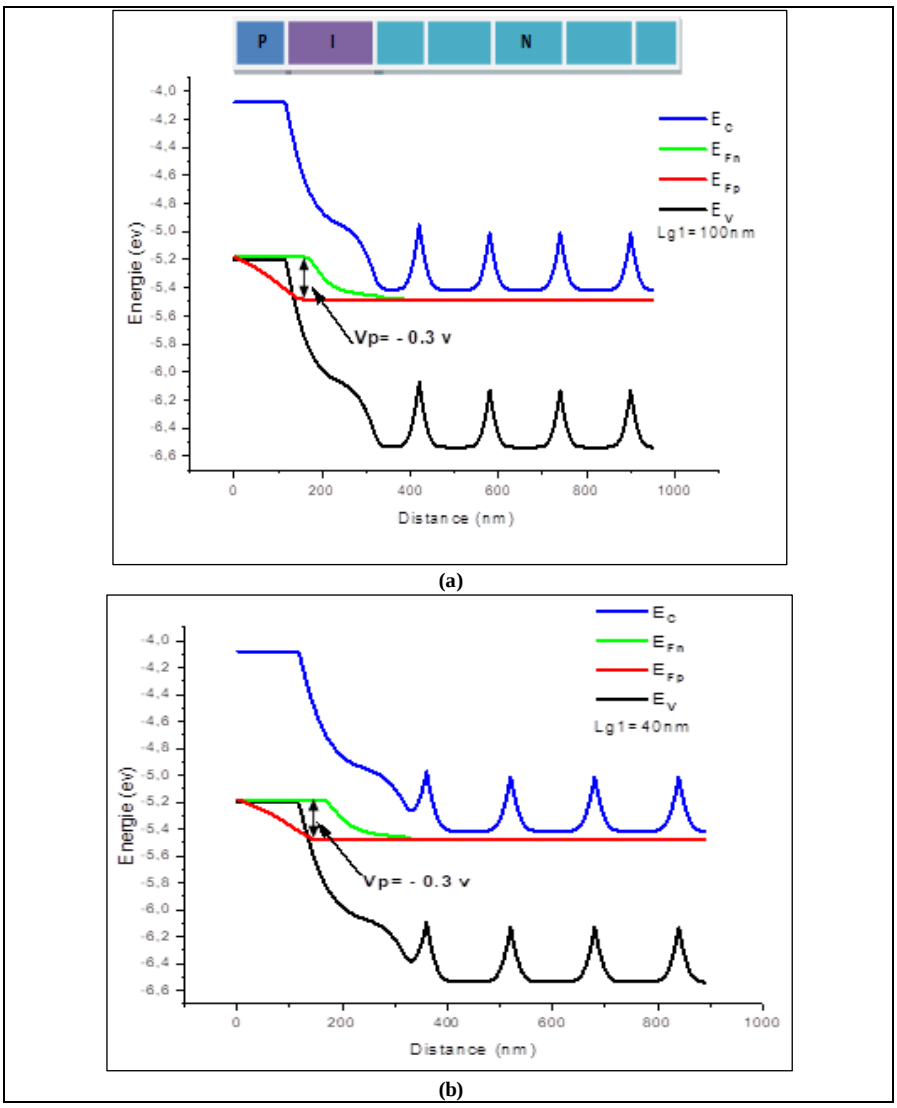

Figure 2: Energy band structures of a polycrystal PIN diode polarized in inverse, with Na=5.1018 cm-3, Nd= 5.1017 cm-3, NT=3.1012 cm-3, Li=200nm, Vp=-0.3.

Source: Authors, (2024).

Like all devices based on polycrystalline silicon, the energy band structures of a polycrystal PIN diode show the crucial role played by the grain boundaries. These boundaries, particularly the first joint parallel grain, block the electrostatic potential and prevent the space charge zone from expanding into the volume of the layer. This blocking effect creates a potential barrier that can only be overcome when a certain reverse voltage is applied. At this point, the first grain boundary's blocking potential is released, and

the subsequent parallel grain boundaries take over the blocking function.

Figure .2a illustrates the energy band structure with a crystallite size Lg=100 nm. The potential barriers created by the grain boundaries are evident, showing how these boundaries impede the flow of carriers, particularly under reverse bias conditions.

Figure .2b depicts the energy band structure with a reduced crystallite size Lg1=40. The smaller grain size results in a higher density of grain boundaries, which further influence the distribution of the electrostatic potential across the device.

These figures highlight the significant role of grain boundaries in shaping the electrical characteristics of polycrystalline silicon PIN diodes. The grain boundaries not only trap free carriers but also create potential barriers that affect the movement of charge carriers, particularly under reverse bias conditions. This understanding is critical for designing more efficient and reliable polycrystalline silicon-based electronic components.

VI. TWO-DIMENSIONAL DISTRIBUTION OF ELECTROSTATIC POTENTIAL

The distribution of electrostatic potential (φ), electron concentration (n), and hole concentration (p) in a PIN diode based on polycrystalline silicon is obtained by solving a two-dimensional system composed of Poisson's equation and the continuity equations for electrons and holes. The parameters for this simulation include Na=5.10^{18} cm^{-3}, Nd= 5.10^{17} cm^{-3}, NT=3.10^{12} cm^{-2}, Lg=160nm, Lg1=100nm, Li=200nm, Vp=-0.3.

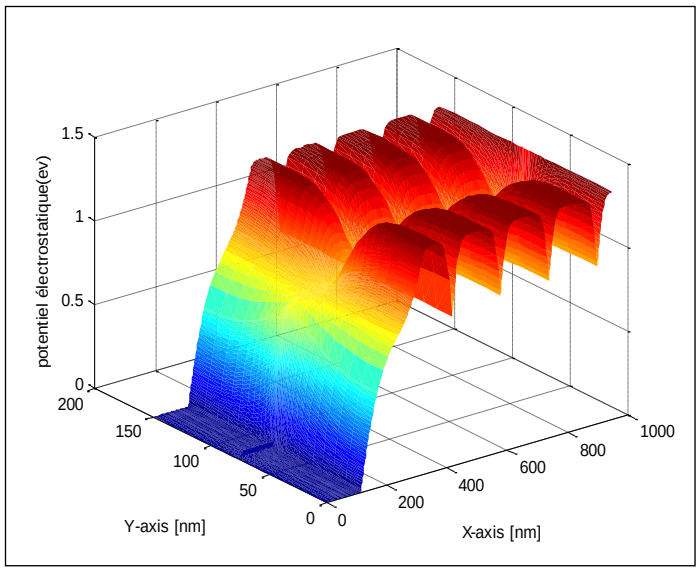

Figure 3: Distribution of the electrostatic potential.
Source: Authors, (2024).

The variation of the electrostatic potential shown in Figure 3 indicates that in the highly doped P+ region, the potential perpendicular to the grain boundary has a negligible effect, characterized by a low intergranular barrier height. Conversely, in the less doped N region, the barrier height due to the metallurgical junction is proportional to the reverse voltage Vp. Near the metallurgical junction, the intergranular barrier height does not depend on the applied field and reaches its maximum at the intersection of grain boundaries. The potential barriers created by these grain boundaries form deserted areas on both sides, limiting the passage of free carriers from one crystallite to another.

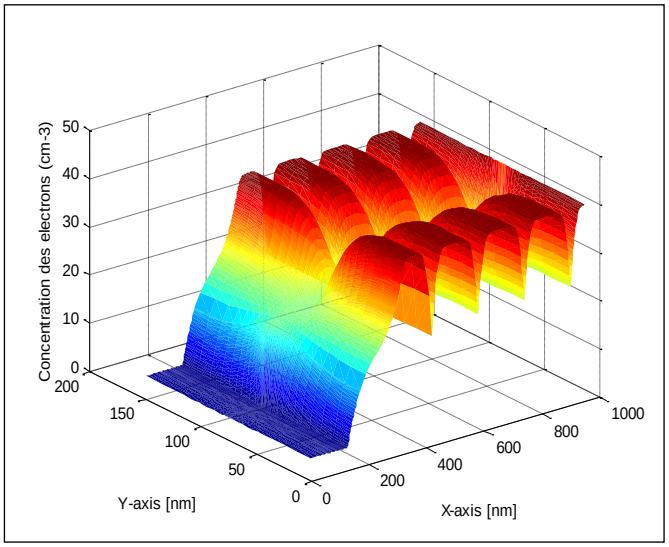

Figure 4: Semi-logarithmic concentration distribution of electron
Source: Authors, (2024).

Using Figure 4, which represents the distribution of free electrons n(x,y) in the device, we observe that the majority of electrons in the N region are trapped due to the high density of acceptor traps in the grain boundaries (NT=3.10^{12} cm^{-2}).Consequently, a significant concentration of electrons compared to the dopant (Nd=$5.10^{17}cm^{-3}$) is observed, indicating that the crystallites are partially depleted of free carriers.

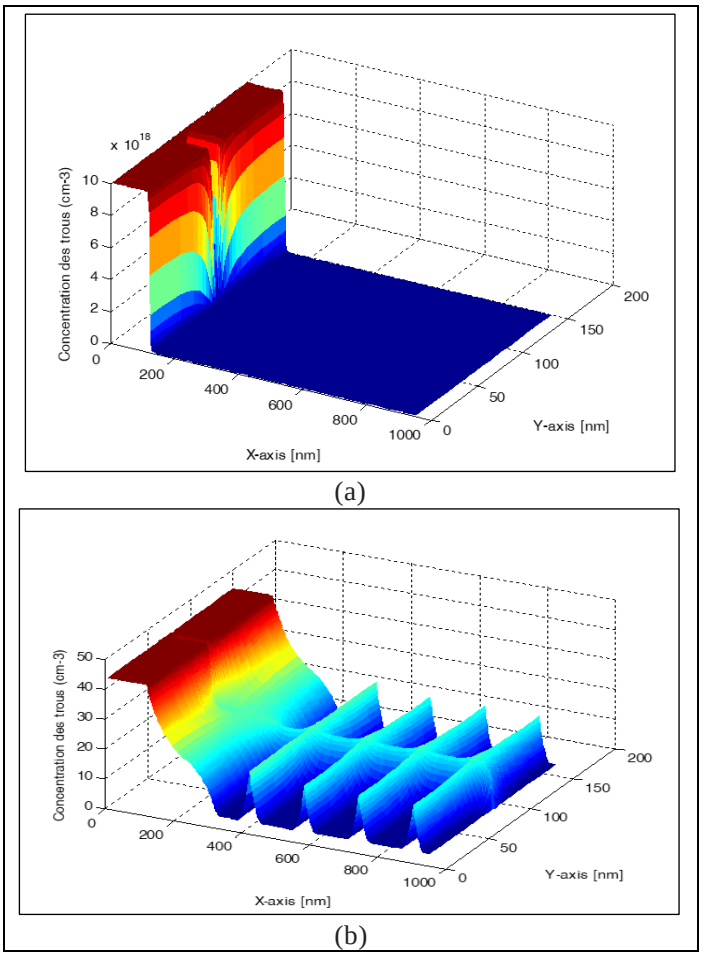

Figure 5: The concentration of holes, linear distribution (a), semi-logarithmic (b).
Source: Authors, (2024).

Figure .5 illustrates the concentration distribution of holes in the device. In the P+ region, electrons are minority carriers, making their concentration negligible compared to that of the dopant. Similarly, holes, which are minority carriers in the N region, become the majority carriers in the P+ region. This transition is depicted in both the linear and semi-logarithmic plots, showing how carrier concentrations vary across different regions of the diode.

VII. INFLUENCE OF GRAIN JOINTS ON REVERSE CURRENT

The variation of current as a function of the reverse voltage (VP) between polycrystalline silicon and monocrystalline PIN diodes is depicted in Figure 6. The parameters for this analysis include (NA =5.1019 cm^{-3}, ND = 5.1017 cm^{-3}, NT = 3.1012 cm^{-2}, Lg=160 nm, Lg1=100 nm).

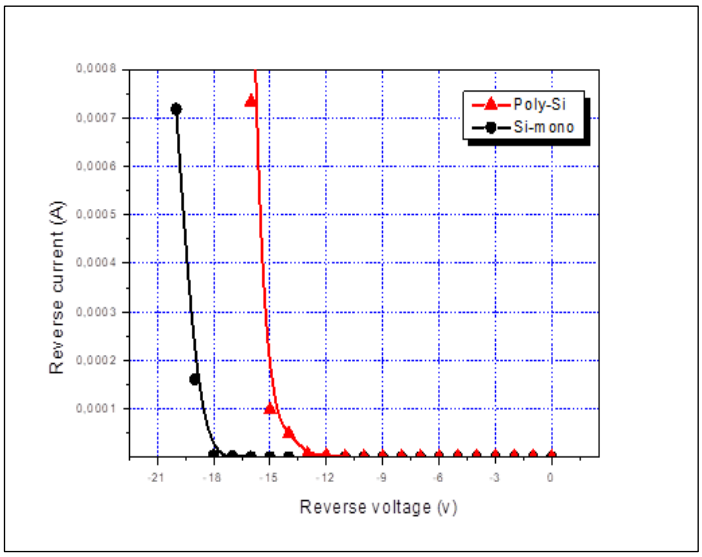

Figure 6: Current-voltage characteristic in the polycrystalline and monocrystalline PIN diode.
Source: Authors, (2024).

The graph shows a clear distinction between the breakdown voltages of the two types of diodes. The polycrystalline silicon PIN diode exhibits a breakdown voltage of approximately 12V, whereas the monocrystalline silicon PIN diode shows a higher breakdown voltage of around 18V. This significant difference indicates that the avalanche breakdown occurs more rapidly in the polycrystalline diode compared to the monocrystalline one.

This behavior can be attributed to the presence of grain boundaries in the polycrystalline material, which contain trap states that reduce the breakdown voltage. The grain boundaries trap free carriers, creating a larger space charge region compared to the metallurgical junction alone. For impact ionization to occur, a high electric field and a sufficient space charge region are necessary to accelerate carriers, thereby generating electron-hole pairs through impact ionization. These newly generated pairs further accelerate, creating more pairs and leading to the avalanche phenomenon.

The difference in breakdown behavior between the polycrystalline and monocrystalline diodes is primarily due to the presence of grain boundaries in the polycrystalline film. These boundaries facilitate the trapping of carriers, thus lowering the breakdown voltage and accelerating the avalanche breakdown process.

VIII. CONCLUSION

This study has provided a comprehensive simulation and analysis of the electrical characteristics of reverse-biased lateral polysilicon PIN diodes, with a particular focus on the effects of grain boundaries and impact ionization. By numerically solving the system of partial differential equations, including Poisson's equation and the continuity equations for electrons and holes, we obtained detailed current-voltage (I-V) characteristics of these diodes.

Our findings reveal a significant difference in the breakdown voltages between polycrystalline and monocrystalline silicon PIN diodes, with the former exhibiting a lower breakdown voltage of 12V compared to 18V for the latter. This difference is primarily due to the presence of grain boundaries in the polycrystalline material, which contain deep energy states that trap free carriers, thereby reducing the breakdown voltage and accelerating the avalanche breakdown process.

The grain boundaries in polycrystalline silicon play a critical role in shaping the diode's electrical behavior. These boundaries create potential barriers that impede carrier movement and contribute to a larger space charge region, which is essential for the onset of impact ionization. The presence of traps at these boundaries facilitates carrier trapping and recombination, further influencing the breakdown characteristics.

The results of this study have important implications for the design and optimization of polysilicon-based electronic components. Understanding the impact of grain boundaries on the electrical properties of polycrystalline silicon diodes can lead to better control of device performance and reliability. For instance, strategies to minimize the adverse effects of grain boundaries, such as improving crystallite size uniformity or optimizing doping levels, could enhance device efficiency and durability.

Moreover, the insights gained from this simulation study can be applied to a broader range of semiconductor devices that utilize polycrystalline materials, including photovoltaic cells and thin-film transistors. Future work could involve experimental validation of the simulation results, as well as the exploration of alternative materials and structures that may offer improved performance characteristics.

In conclusion, this study underscores the critical importance of grain boundaries in determining the electrical characteristics of polycrystalline silicon PIN diodes. By providing a detailed understanding of these effects, we contribute to the advancement of semiconductor technology and the development of more efficient and reliable electronic devices.

IX. AUTHOR'S CONTRIBUTION

Conceptualization: Abdelaziz Rabehi, Abdelmalek Douara, Mohamed Elbar.
Methodology: Abdelaziz Rabehi, Abdelmalek Douara, Mohamed Elbar.
Investigation: Abdelaziz Rabehi, Abdelmalek Douara, Mohamed Elbar, Roumaissa Zenzen and Mohamed Amrani.
Discussion of results: Abdelaziz Rabehi, Abdelmalek Douara, Mohamed ELBAR, Roumaissa Zenzen and Mohamed Amrani.
Writing – Original Draft: Abdelaziz Rabehi, Mohamed Elbar.
Writing – Review and Editing: Abdelaziz Rabehi, Abdelmalek Douara, Mohamed Elbar.
Supervision: Abdelaziz Rabehi, Abdelmalek Douara, Mohamed Elbar, Roumaissa Zenzen and Mohamed Amrani.

Approval of the final text: Abdelaziz Rabehi, Abdelmalek Douara, Mohamed Elbar, Roumaissa Zenzen and Mohamed Amrani.

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