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RESEARCH ARTICLE OPEN ACCESS

FAULT DIAGNOSIS AND FAULT TOLERANT CONTROL STRATEGY FOR INTERLEAVED BOOST DC/DC CONVERTER DEDICATED TO PEM FUEL CELL APPLICATIONS

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ABSTRACT

This paper proposes an improved fault diagnosis and fault tolerant control (FTC) strategy for interleaved boost DC/DC converter that is suitable for fuel-cell applications. This paper investigates a two-phase interleaved boost DC-DC converter. This design offers several advantages, including: Low ripple current, by splitting the load current between two phases, the ripple current at the input and output is significantly reduced compared to a single-phase converter. Reduced semiconductor stress, Each phase handles only a fraction (1/N) of the total current, which reduces stress on individual components and promotes higher reliability and operating margins. Furthermore, the paper proposes and evaluates an H-infinity controller for the converter. This advanced control strategy ensures robust performance despite variations in reference voltage and load conditions. The power converter suffers from failure switching due to various factors. To address these drawbacks and achieve both accurate reference tracking with desired dynamic response and rapid fault detection, an algorithm based on current-slopes are proposed. Minimizing current ripples is crucial to ensure the longevity of PEMFCs, so the interleaved boost converter structure is dedicated to the PEMFCs in order to reduces the ripple of the generated current. The overall system has been simulated using MATLAB/Simulink software under different conditions such as reference voltage variation, load variation, and Short Circuit default; the obtained results in different phase demonstrate the higher performance, of the proposed systems in terms of dynamic performance, fast fault detection and fault tolerant action to restore the health stat.

I. INTRODUCTION

PEMFCs offer a compelling future for environmentally friendly sustainable power generation, particularly in aviation, automobiles, and shipping. Their appeal lies in several key advantages: minimal environmental pollutants, quiet operation, low operating temperatures, and high efficiency. [1-2].

The PEMFC system exhibits a non-linear relationship between voltage and current (V-I) [3]. The voltage and current are directly proportional to the generated power level.

Undoubtedly, fluctuations in current have been demonstrated to negatively impact the operational lifespan of Polymer Electrolyte Membrane Fuel Cells (PEMFCs). To address this, integrating a power interface necessarily required. This interface serves two key purposes: stabilizing the output voltage and mitigating current ripples by employing a DC-DC converter, we can effectively regulate the FC output voltage, eliminating inconsistencies and protecting the PEMFCs, ultimately extending their lifespan [4].A DC–DC converter can be used to adjust the output voltage value of the renewable energy sources (PEMFC) [5] It's essential to minimize the ripple current in the PEM fuel cell. [6]

Furthermore, several control strategies have been employed for interleaved converters, each with its own advantages and limitations. PI control based on the average model is a simple and popular approach, but it can be less effective at handling nonlinearities and varying operating conditions [1]. In [7-9] a linear quadratic mode controller is designed this method offers improved robustness against disturbances.

Semiconductors are much more likely to fail than in other application areas, with over 30% of switch failures. These failures can be broadly grouped into two types: short circuit faults (SCF) and open circuit faults (OCF). Because of this, early fault diagnosis is crucial for finding and fixing switch failures. [10]

In [11] deals with open switch faults detection and localization in shunt active three-phase filter based on two level voltage source inverter [11].

In [12] focus on the diagnosis of short-circuited turns fault in BLDC motors. The proposed approach is based on residual generation using a first order sliding mode observer which has been widely used for BLDC sensorless control.

In [13] focuses on define the fault classification and then give an example of modeling and introduce a fault detection method to detect the assumed faults.

A switch fault diagnosis technique based on a Luenberger observer is presented in [14] for the dc-dc interleaved boost converter for fuel cell (FC) application.

Shahbazi. et al. [15] has investigated FD in non-isolated dc-dc converters using FPGA. The sign of the input current slope and switch gate edge type are used to detect the fault.

Firstly, this paper present a comparative study between a simple PI controller and H∞ robust controller of an interleaved boost converter in order to Current ripple reduction from the PEM Fuel cell and to Tight output voltage regulation at the required value without failure mode.

Secondly, this paper proposed a new algorithm fault detection in dc-dc boost converter based on input current slope for Short Circuit power switch failure mode and fault tolerant actions to restore healthy state.

This paper is organized into three section areas: Section 2 Introduces the Proton Exchange Membrane Fuel Cell (PEMFC). In section 3, Explores the DC-DC boost converter, delving into its presentation and modeling. In section 4, Focuses on the interleaved boost DC-DC converter, providing details and its presentation. In section 5 focuses on the development of an algorithm for the diagnosis of switch failures. The proposed algorithm aims to enhance converter resilience and availability through early detection of switch malfunctions.

Presents and discusses the simulation results obtained for the proposed the control for interleaved boost converter ‹The discussion covers both healthy and failed operational conditions, providing valuable insights into its performance and robustness in section 6.

Finally, Key findings and insights are summarized and the paper's most significant contribution in the concluding section 7.

II. PEMFC PRESENTATION

In this section, the mathematical model is derived for a fuel cell stack

We'll unravel the key chemical reactions at the anode, cathode, and within the entire process, laying the foundation for understanding the precise equations that govern this technology.

Anode:

$$H{=}2H^{+} + 2e^{-} \qquad (1)$$

Cathode:

$$\frac{1}{2}O_2 + 2H^{+} + 2e^{-} = H_2O \qquad (2)$$

Global reaction:

$$H_2 + \frac{1}{2}O_2 = H_2O \qquad (3)$$

Figure 1 presents the single cell's static V-I polarization curve, The significant voltage drop in Fig. 1 is stack voltage stems from three primary losses, Notably, at low current levels, ohmic loss becomes negligible and the voltage rise primarily results from slower chemical reactions. This region is aptly named "activation polarization." At very high current density the voltage plummets considerably due to diminished gas exchange efficiency.[9-16],[17]

$$V_{FC} = E - V_{ac} - V_{ohm} - V_{con} \qquad (4)$$

Where:

VFC : Open-circuit voltage of PEMFC
E : thermodynamic voltage
Vac : activation losses
Vohm : ohmic losses
Vcon : concentration losses

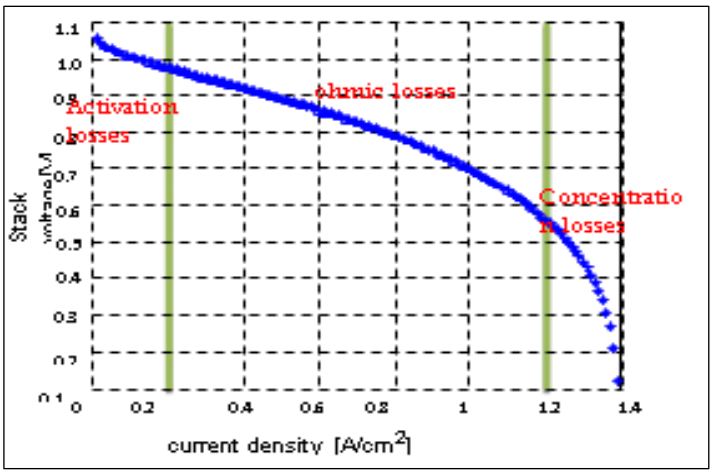

Figure 1: V-I characteristic of a PEM fuel cell.
Source: Authors, (2025).

The distributed nature of phase interleaving allows the converter to manage higher currents, making it ideal for high-power applications thanks to its unique structural advantages [18].

III. MODELING AND CONTROL OF DC-DC BOOST CONVERTER

III.1 MODELING OF BOOST CONVERTER

In the realm of power electronics, the DC-DC boost Converter plays a crucial role by takeing a lower DC voltage to a higher, desired level. As illustrated in Figure 2 the converter is showed.

The DC-DC boost converter comprises several key components: an inductor, a MOSFET switch, a rectifier diode, and an output capacitor. The inductor acts as an energy reservoir, storing energy during the switch's ON-time and releasing it when the switch is OFF. The switch control the converter ON or OFF; the diode element enforces unidirectional energy flow, and the output capacitor stores to deliver stabilized power to the load [19].

The duty cycle of the boost converter is generally controlled via pulse width modulation (PWM).[20].

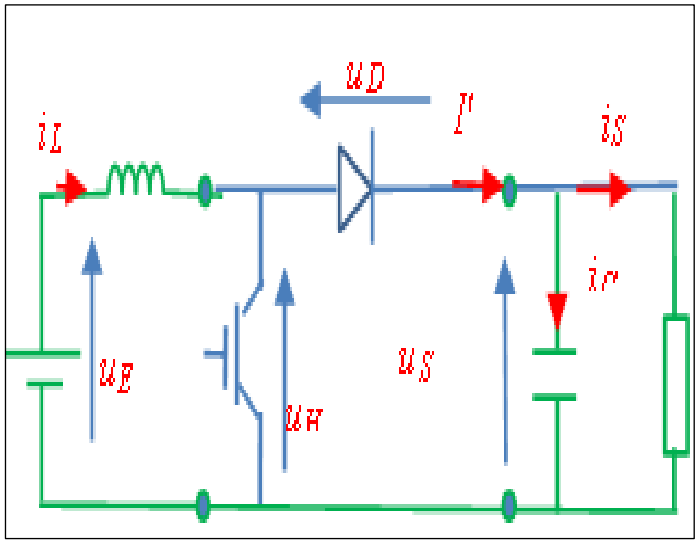

Figure 2: fundamental schematic of a DC-DC boost converter.
Source: Authors, (2025).

Let's analyze the DC-DC converter's governing equation. Specifically, let's identify the model.

$$\begin{cases} \frac{di_L}{dt} = \frac{1}{L}(U_E - U_H) \\ \frac{du_S}{dt} = -\frac{1}{RC}u_S + \frac{1}{C}I' \end{cases} \quad (5)$$

We calculate the mean values of the voltages and currents:

$$\begin{cases} U_H = \frac{1}{T}\int_{\alpha T}^{T} U_S\, dt = \frac{U_S}{T}(T - \alpha T) = u_s(1-\alpha) \\ I' = \frac{1}{T}\int_{\alpha T}^{T} i_L\, dt = \frac{i_L}{T}(T - \alpha T) = i_L(1-\alpha) \end{cases} \quad (6)$$

By replacing UH, I' in Eq. (5),
The model is:

$$\begin{cases} \frac{di_L}{dt} = -\frac{1-\alpha}{L}u_s + \frac{U_E}{L} \\ \frac{du_s}{dt} = \frac{1-\alpha}{C}i_L - \frac{1}{CR}u_s \end{cases} \quad (7)$$

We can linearize the behavior of the model with the equilibrium point:

$$\begin{cases} u_{s0} = \frac{U_E}{1-\alpha_0} \\ i_{L0} = \frac{U_E/R}{(1-\alpha_0)^2} \end{cases} \quad (8)$$

Applying the Laplace transform to the model in in Eq. (7), we obtain the following representation :

$$\frac{\Delta u_S}{\Delta \alpha} = -\frac{U_E\left[\frac{S}{RC(1-\alpha_0)^2} - \frac{1}{LC}\right]}{\left[S^2 + \frac{S}{RC} + \frac{1}{LC}(1-\alpha_0)^2\right]} \quad (9)$$

III.2 PI CONTROL

The controller employs a proportional gain (Kp) to enhance system dynamics and an integral term with gain (Ki) to ensure accurate steady-state tracking. The PIDTOOL instruction within the direct closed-loop system facilitates the synthesis of these optimal Kp and Ki values. [1] [21]

III.3 H∞ MIXED SENSITIVITY CONTROL DESIGN

A H∞ regulator ensures precise regulation the output voltage of the DC-DC converter as presented in Figure 3.

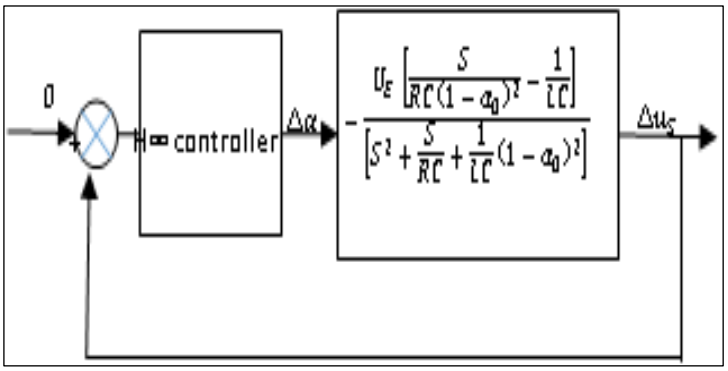

Figure 3: voltage controller.
Source: Authors, (2025).

To impose some dynamical performances in a H∞ control , it is necessary to include some weighting filters. In the proposed design, two weighting filters W1(s) and W2(s) are included in the Plant [22]

The parameters of the H∞ controller are designed using the transfer function given by Eq. (9) as follows:
the weighting function ws(s) is chosen as:

$$Ws(s) = \frac{0.6667*s+495.9}{s+0.002.48}$$

The weighting function Wu2 is defined as:
$Wu(s) = 1$

The "hinfsyn" tools is used to performed the design of the H∞ mixed sensitivity controller K(s).

The H∞ mixed sensitivity current loop controller is described as:

$$K_{\infty Voltage}(s) = \frac{6436*s^2+2.575e06*s+6.436e09}{s^3+7.421e04*s^2+2.733e09*s+8.2e06}$$

IV. INTERLEAVED BOOST CONVERTER PRESENTATION

In a two-phase interleaved converter, the parallel converters switch ON and OFF at staggered times, separated by half the switching period (T/2). Both branches operate with identical duty cycles.

The average model of the IBC is the same as the conventional boost DC-DC converter the IBC's distinct characteristic is the presence of two current inductors.

Interleaved boost converters (IBCs) enable high current flow while significantly reducing input current ripple. Figure 4 illustrates the IBC topology.

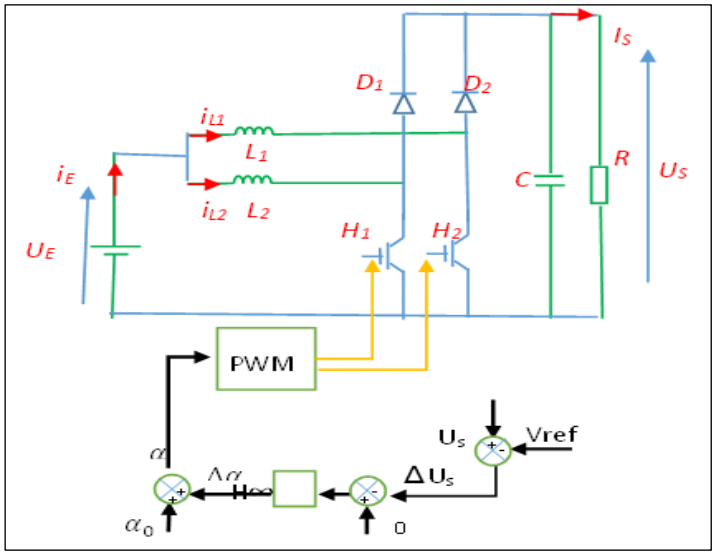

Figure 4: DC-DC Interleaved boost converter.
Source: Authors, (2025).

V. FAULT DIAGNOSIS

We propose a new general fault detection method for the conversion DC to interleaved DC, based on an algorithm to detect any type fault open-circuit (OCF) or short-circuit (SCF) occurring at the switch orderable. The algorithm is based on observing the waveform of the current flowing through the inductor. We mention right now that this algorithm is very fast and is robust and effectively detects all types of faults in all conditions.

Fault detection is a two-step process involving fault time logging and fault alarm generation. Subsequent to these steps, automatic restoration mechanisms are employed to enable the process to recover its secure operational state. [23]

This method characterized by:

- high robustness
-very fast for Detection
-low Implementation Effort
- low cost
- Do not depend on load

This algorithm is based on the following principle (see Figure **5**):

Normal operation, when the SW controllable switch is closed, the current at through the inductance (iL) then increases that when the same switch is opened, the Current iL decreases. the current slope sign iL changes simultaneously with the command order of the SW switch. In practice, in particular because of the effects of switching and SW driver downtime, there is a Td delay between the order change of control of the SW switch and its effective change of state.

We would like to point out here that it is not useful to know the exact value of diL/dt, but only its sign. So, we can use a simple and effective method so that the fault detection process is not too complex and does not require too much processing time, to the detriment of the temporal performance of the detection method.

Since our method is intended to be implemented digitally, we propose estimate the length of time that the err signal is equal to '1' (under normal operation, this duration is denoted Ts in Figure 6). We then built the detection offered on a signal called Trig. This signal consists of a series of pulses of short duration (equal to Ts), equal to '1' and generated at the beginning of each operation, when switching to '1' of the signal. After each pulse of the Trig signal, the current in the inductance must then increase, and then decrease. If this current iL is always increasing or decreasing between the two pulses of the Trig signal, it can be concluded that a fault has occurred. A counter, shown on the Figure 6 shows this duration, quantified in terms of the number of periods sampling Ts" and denoted nc. When the err signal is equal to '1', the nc output of The counter increments with each clock rising edge (active edge). The value of nc is reset after each descending edge of the err signal. The resulting nc signal is a "Sawtooth" type signal. The maximum value achieved is directly related to two quantities: the time during which the err signal is equal to '1' (duration Td, Figure 6) and the value of Ts (Td = nc *Ts).

Next, the nc signal is compared with its N-rated threshold value. This threshold must be greater than the maximum nc value during normal operation of the converter.

The absolute value of the error $|err|$ signal is "constantly monitored": this means that The fault must be executed in parallel with the control algorithm of the converter. If this err signal remains in the '1' state for a longer period of time than NTc, we concludes that there is a failure. In Figure 6, we can visualize the Schematic representation of fault detection by the FD algorithm. This block has an output (FD), three nc, $|err|$ and SdiL inputs, one clock input and one Reset (Rst) input for reset. [24]

From these two sampled values of the current iL ,the SdiL1 function is compare the current slope to zero:

If the dIL1 is positive, the SdiL1 is 1
Else the SdiL1 is equal 0, We can So write:

$$\begin{cases} S\ \frac{di1}{dt} = 1\ t\epsilon[0, DT_s] \\ S\ \frac{di1}{dt} = 0\ t\epsilon[DT_s, T_s] \end{cases} \quad (9)$$

The difference between SdiL1 and State Switch K1, gives us the absolute value of the error $|err|$:

$$|err| = \text{State Switch K1 - SdiL1} \quad (11)$$

In normal operation, without failure, we must have:

$$Td < nc * Ts \quad (12)$$

After the fault detection, and its isolation, the proposed control reconfiguration methodology implements corrective actions, enabling the DC-DC Interleaved Boost Converter to resume pre-fault operation. Simulations in MATLAB/Simulink validate the approach's effectiveness. Notably, the suggested algorithm is simple, and easy configurability.

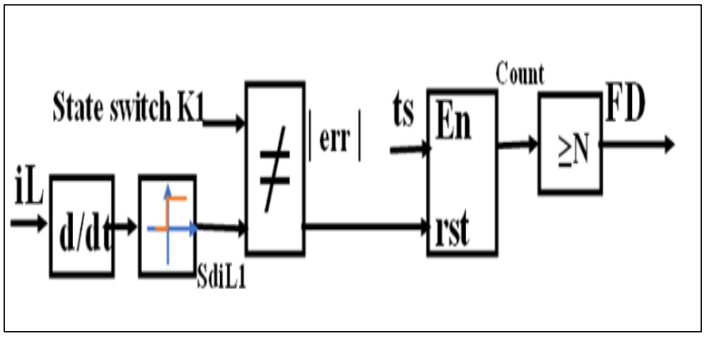

Figure 5: Switch fault diagnosis based on FD algorithm.
Source: Authors, (2025).

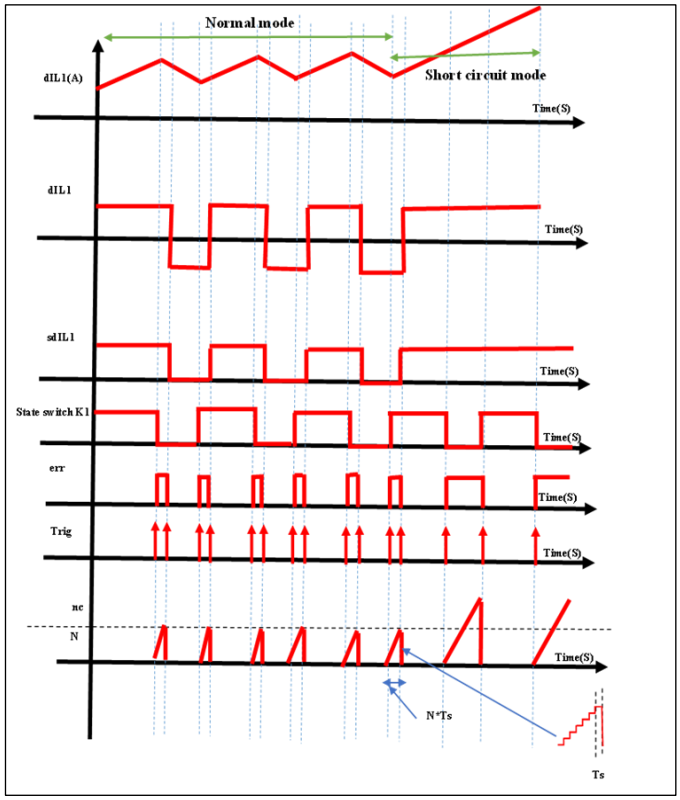

Figure 6: Main signals of the DF algorithm during a under short circuit fault.
Source: Authors, (2025).

VI. RESULTS AND DISCUSSIONS

The Table I below outlines the parameters of a DC-DC interleaved boost converter, The following subsections evaluate and compare the performance of each controller.

Table 1: DC-DC interleaved boost converter parameters.

PARAMETERS	E	L1	L2	C	F	R
VALUE	40 V	5MH	5MH	50 μ F	20 KHZ	50 OHMS

Source: Authors, (2025).

The Values of the parameters of the H∞ and PI controllers are given in Table II

Table 2: parameters of the controllers.

SWITCHING FREQUENCY	20 KHZ
KP	0.00037088
KI	0.4619
WS(S)	(0.4*S+180)/(S+0.003)
WU(S)	1

Source: Authors, (2025).

VI.1 VARIABLE REFERENCE OUTPUT VOLTAGE

The H∞ controller effectively regulates the system for both transient and steady-state conditions, as demonstrated in Figure 7, Increasing the reference output voltage, also shown in Figure 7, results in a proportional increase in IBC currents iL1, iL2, and iL depicted in Figure 8 and Figure 9 respectively.

The interleaved boost structure effectively reduces the absorbed current ripple. The IBC design ensures consistently low current ripple across different output voltage phases, regardless of fluctuations in the output reference voltage (as demonstrated in in Figure 9). Notably, Figure 10 illustrates the corresponding duty cycle behavior, where higher reference voltages translate to increased duty cycle values.

The state commutation of switch K1 is clearly 20 kHz, as illustrated in Figure 11.

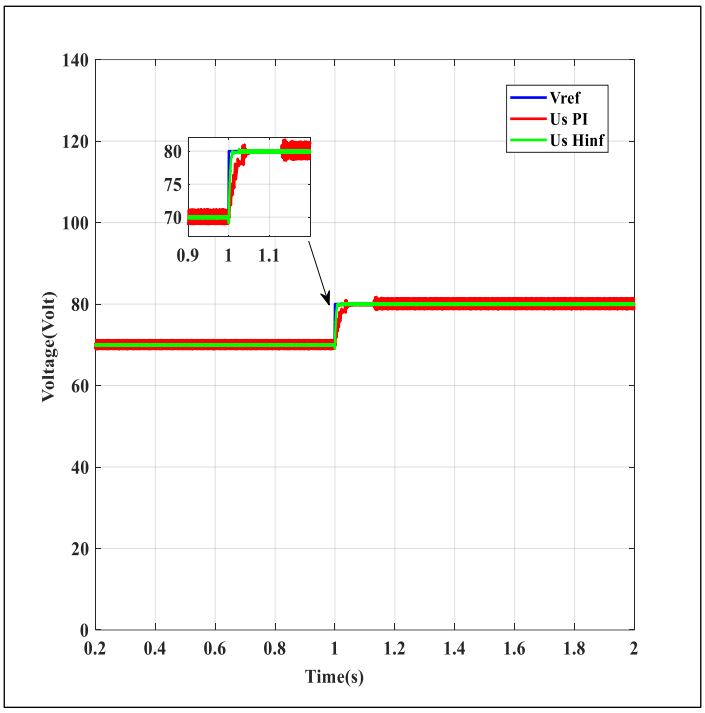

Figure 7: output voltage of the DC-DC converter under voltage variation.
Source: Authors, (2025).

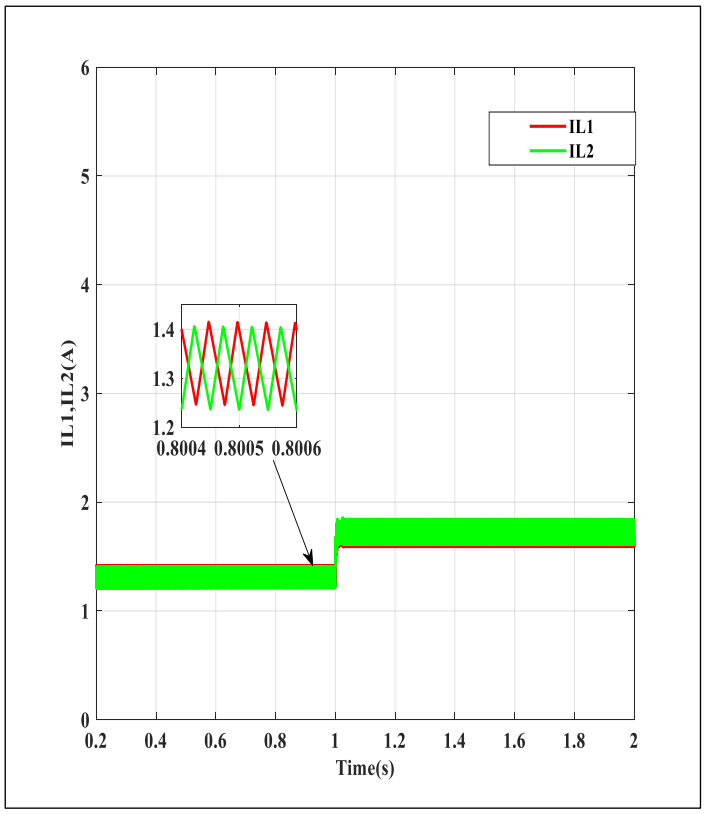

Figure 8: Waveform of branch currents iL1, Il2 under voltage variation.
Source: Authors, (2025).

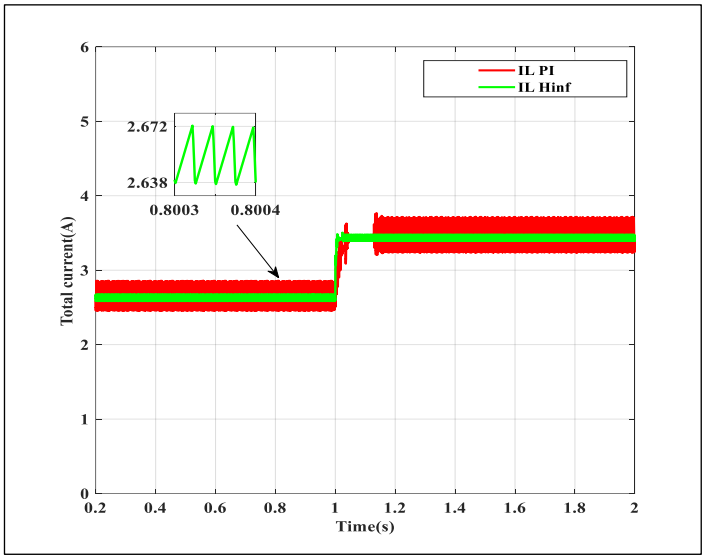

Figure 9: Waveform of total current under voltage variation.
Source: Authors, (2025).

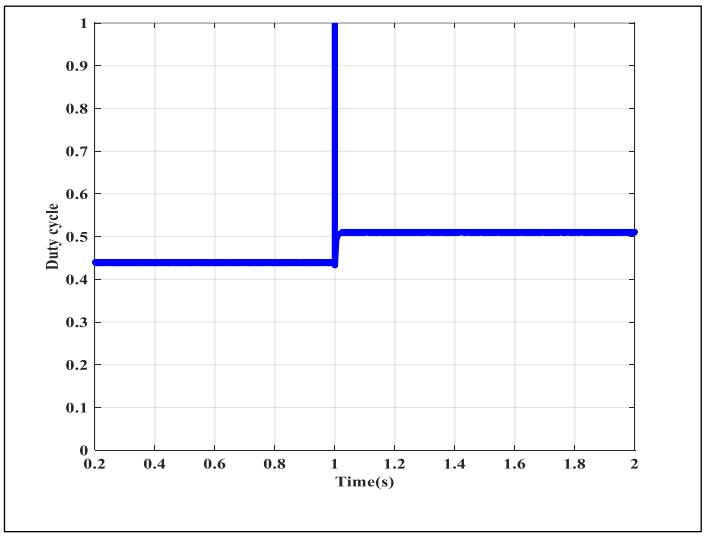

Figure 10: Duty cycle evolution under voltage variation.
Source: Authors, (2025).

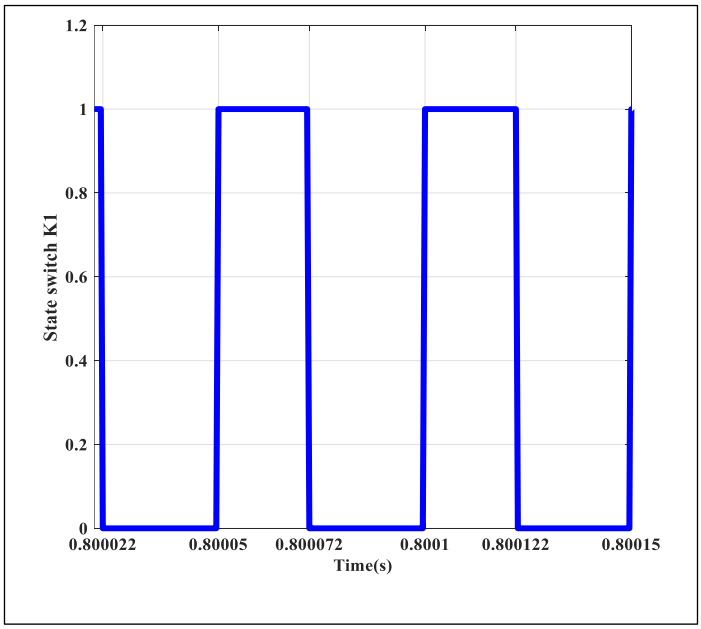

Figure 11: State Switch commutation.
Source: Authors, (2025).

VI.2 FAULT DETECTION METHOD

This section outlines the different steps involved in the proposed fault detection method implemented using MATLAB/Simulink.

Firstly, a Short-Circuit Fault (SCF) is simulated on the first power switch of a two-stage interleaved boost converter. This is achieved by connecting a normally- off ideal switch in parallel with the first switch, which switch-on at tfault =7ms, effectively short-circuiting the switch Figure 12 depicts the system's response under the simulated SCF scenario.

It is obvious that the converter structure is fault tolerant. We can only note a minor degradation in performance.

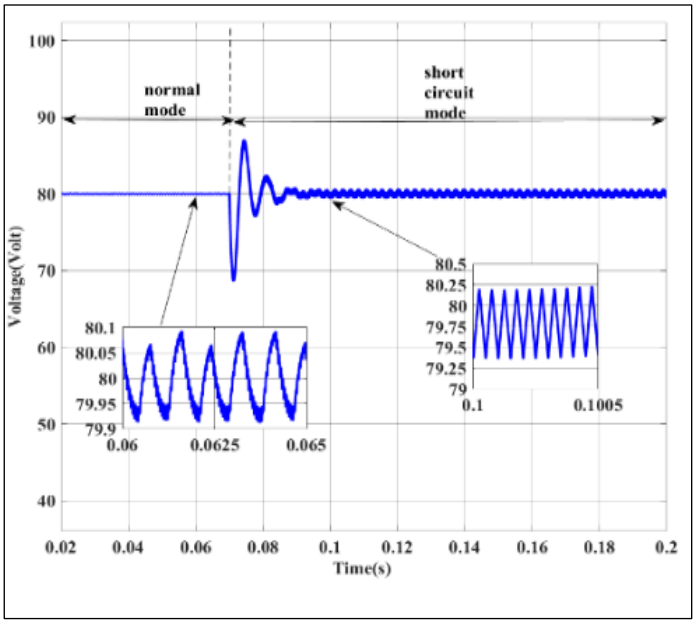

Figure 12: output voltage of the DC-DC converter under short circuit fault.
Source: Authors, (2025).

Figure 13 shows the evolution of currents iL1 , iL2 and iL , before and after the fault.

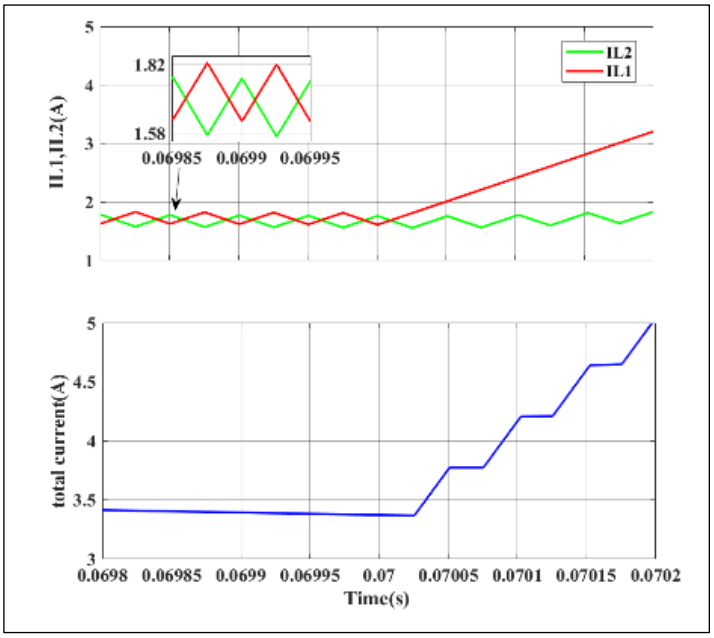

Figure 13: Waveform of IL1, Il2 and IL under short circuit fault.
Source: Authors, (2025).

The process of fault detection using the proposed method is described in detail in the following simulation results.

Figure 14 shows the control signal. the difference between the diL1 current derivation signal and the switch 1 control signal represents the time required for the switch to be opened or to be closed. see Figure 14 (healthy mode).

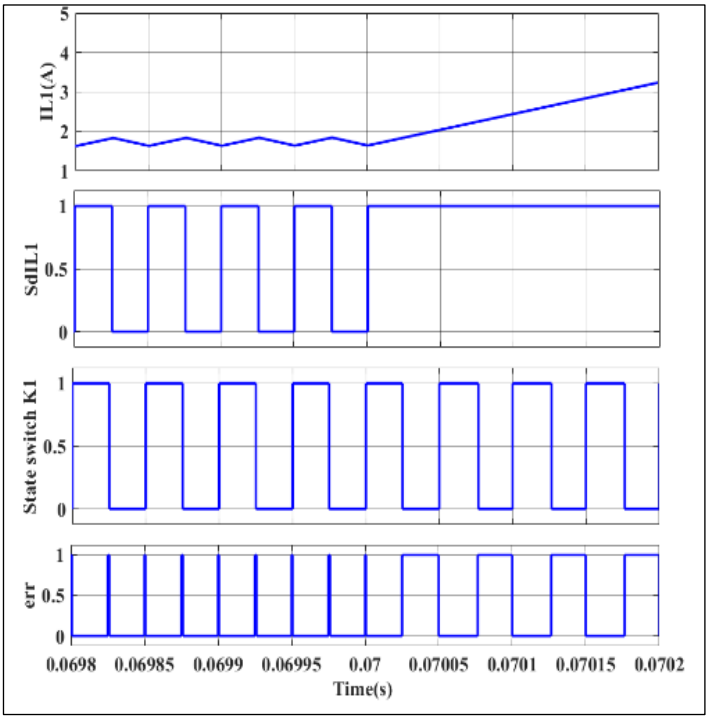

Figure 14: Waveform of IL1, sdIL1,state switch K1 and err under short circuit fault.
Source: Authors, (2025).

A counter is used to convert the time required to open or close the power switch into N*Ts (see Figure 15).
This N*Ts must not exceed 20 microseconds (normative delay). if this time is exceeded, the fault is detected as shown in Figure 16.

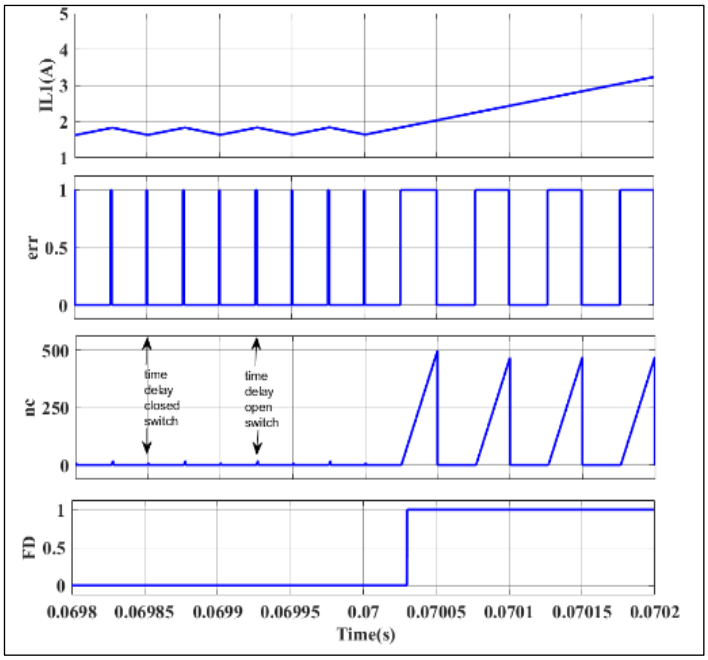

Figure 15: Waveform of IL1, err, nc and FD under short circuit fault.
Source: Authors, (2025).

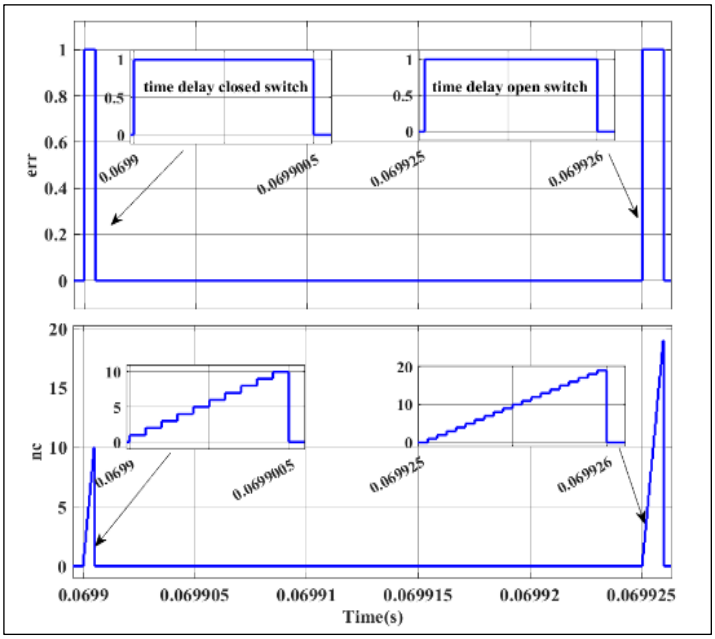

Figure 16: Waveform of the time required to open or close the power switch.
Source: Authors, (2025).

Normal operation, we note that (the time delay closed circuit is deferent for the time delay open circuit (Td_closed=5e-7s, Td_open=1e-6s)

VI.3 FTC FOLLOWING A DCC DETECTED BY DF ALGORITHM (R= 50)

A fault tolerant control is used in the event of a fault being detected, which consists of isolating the faulty converter stage. Figure 17 shows the evolution of currents iL1 and iL2. In the event of a fault on power switch 1, stage 1 is isolated (iL1 becomes zero as shown in Figure 17).
we note only a minor degradation in performance.

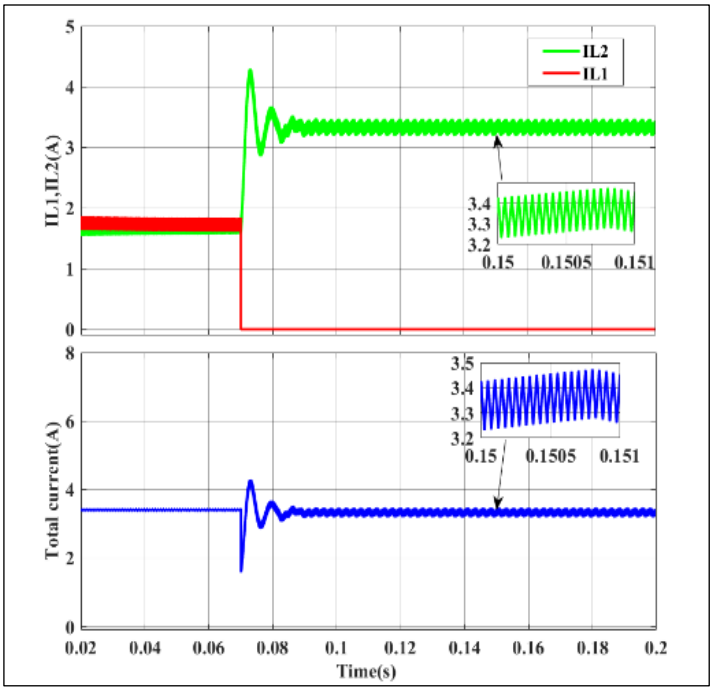

Figure 17: Waveform of IL1, IL2 and IL under fault tolerant control.
Source: Authors, (2025).

V. CONCLUSIONS

In this paper a fault diagnosis and fault tolerant control (FTC) strategy for interleaved boost DC/DC converter is discussed. The structure proposed allows the reduction of the undulation of the current delivered by the PEMFC, and the reduction of the stresses on the semiconductors.

Also, this paper introduces a technique based on H∞ controller used to regulate the output voltage of the interleaved boost DC/DC converter operating in continuous conduction mode. After converter modeling and H∞ controller design, MATLAB/Simulink simulations were conducted to evaluate controller performance under varying desired output voltages and load conditions.

Also, this paper proposes a new general fault detection method based on an algorithm to detect any type fault open-circuit (OCF) or short-circuit (SCF).

The algorithm is based on observing the waveform of the current flowing through the inductor.

As a final conclusion, that the proposed system offers good performances under different conditions such as reference voltage variation and Short Circuit default. The obtained results in different phase demonstrate the higher performance, of the proposed systems in terms of dynamic performance, fast fault detection and fault tolerant action to restore the health stat.

VI. AUTHOR'S CONTRIBUTION

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