Journal of Engineering and Technology for Industrial Applications

ITEGAM-JETIA

Manaus, v.12 n.57, p. 16-23. January/February, 2026.

DOI: https://doi.org/10.5935/jetia. v12i57.2646

ISSN ONLINE: 2447-

RESEARCH ARTICLE OPEN ACCESS

MULTI-OBJECTIVE OPTIMIZATION OF CMOS FOLDED-CASCODE OTAS USING DIVERSE EVOLUTIONARY ALGORITHMS

Pankaj P. Prajapati[1], Alpesh M. Patel[2*], Anilkumar J. Kshatriya[3], Kirit V. Patel[4], Ghanshyamkumar Sah[5], Chintan Dave[6], Kinjal R. Sheth[7], Devendra H. Patel[8]

[1,6,7]Electronics and Communication, Vishwakarma Government. Engineering College, Ahmedabad, Gujarat, India.
[2,3,4]Electronics and Communication, Government Engineering College, Gandhinagar, Gujarat, India
[5]Electronics and Communication, L. D. College of Engineering, Ahmedabad, Gujarat, India.
[8]Electronics and Communication, Government Engineering College, Patan, Gujarat, India.

[1]http://orcid.org/0000-0001-6731-4264, [2]http://orcid.org/0000-0001-8846-4771, [3]http://orcid.org/0000-0002-9044-0442, [4]http://orcid.org/ 000-0002-1280-9937, [5]http://orcid.org/0009-0009-4049-2410, [6]http://orcid.org/0009-0002-1082-7928, [7]http://orcid.org/0000-0003-0132-3533, [8]http://orcid.org/ 0009-0000-8222-6684

Email: pankajprajapati@vgecg.ac.in, *am_patel@gtu.edu.in, anil@gecg28.ac.in, kirit@gecg28.ac.in, ghanshyam@ldce.ac.in, cb_dave@gtu.edu.in, kinjalsheth@vgecg.ac.in, pateldevendrah@gmail.com

ARTICLE INFO

Article History
Received: September 2, 2025
Revised: November 20, 2025
Accepted: January 1, 2026
Published: January 31, 2026

Keywords:
EA,
DE algorithm,
PSO algorithm,
CS algorithm,
Optimization.

ABSTRACT

The manual development of CMOS-based analog circuits continues to pose significant challenges, largely due to device scaling, process-induced variations, and the nonlinear interactions among multiple interdependent design parameters. These complexities necessitate the advancement of automated methodologies to improve efficiency, scalability, and reliability in analog design. In this study, the Cuckoo Search (CS) algorithm is investigated as a robust evolutionary framework for the automated sizing of CMOS analog circuits, with particular emphasis on the Folded Cascode Operational Transconductance Amplifier (FOTA) implemented in both 0.18 µm and 0.35 µm CMOS technologies. To provide a rigorous comparative analysis, the performance of CS is benchmarked against two widely employed evolutionary algorithms, namely Differential Evolution (DE) and Particle Swarm Optimization (PSO). All algorithms were implemented in the C programming language, interfaced with the NGSPICE simulator, and executed on an Intel® Core™ i5 processor (2.40 GHz, 8 GB RAM) under the Ubuntu operating system. The experimental findings reveal that CS consistently exhibits superior performance in terms of success rate, convergence reliability, and robustness. Specifically, in the case of the 0.35 µm FOTA design, CS achieved convergence to all target specifications in 9 out of 10 independent runs, outperforming DE (eight successes) and PSO (five successes). Comparable superiority of CS was also observed for the 0.18 µm process, thereby validating its potential across multiple technology nodes. This study demonstrates that CS not only provides superior optimization outcomes compared to DE and PSO but also establishes itself as a highly effective and reliable evolutionary framework for automated analog circuit design. The cross-technology validation and performance benchmarking highlight its practical relevance in advancing analog design automation

I. INTRODUCTION

CMOS analog circuits form the foundation of systems ranging from precision sensors to high-speed communication links, yet their design remains demanding. Device-level variations, parasitic effects, and nonlinear behavior make analog optimization far more intricate than its digital counterpart. At the same time, designers must reconcile requirements for gain, bandwidth, stability, efficiency, and area, a combination that calls for rigorous multi-objective optimization methods.Among circuit-level challenges, transistor sizing is the most critical. The folded-cascode operational transconductance amplifier (OTA) exemplifies these difficulties: its architecture resolves voltage headroom constraints while retaining high gain, offering wide input range and strong power-supply rejection. Yet its performance is highly sensitive to transistor dimensions, bias allocation, and parasitic interactions. Trade-offs among gain, bandwidth, slew rate, and power dissipation are further complicated by process variation.This study explores evolutionary algorithms (EAs) as a framework for transistor-level optimization, emphasizing their integration with high-fidelity circuit models. Through systematic evaluation, it demonstrates the capacity of EAs to handle the complexity of analog design spaces and to deliver balanced solutions across conflicting performance metrics, thereby advancing the automation and reliability of CMOS analog circuit design.

II. LITERATURE REVIEW

PSO has been widely used for automated sizing of CMOS analog circuits in SPICE-in-the-loop frameworks due to its simplicity, exploratory power, and reliable convergence in complex design spaces. Research has mainly focused on addressing its stagnation tendency and sensitivity to parameter settings. Shreeharsha et al. [1] developed an enhanced-velocity PSO (EV-PSO) with adaptive inertia weight and acceleration factors for CMOS op-amp sizing. The method encouraged broad exploration in the early phase and shifted to precise refinement later, leading to quicker convergence and a larger set of practical solutions than the basic PSO. In high-frequency circuit design, where parasitics and layout effects make optimization difficult, Liu et al. [2] applied a randomized PSO (R-PSO) to the co-design of a 60 GHz subharmonic mixer. Constraint handling is equally critical, since many analog design requirements—such as minimum phase margin or maximum slew rate—are imposed as strict limits rather than soft targets.

Bouali et al. [3] developed a constraint-repaired PSO variant that incorporates adaptive neighborhooding to dynamically adjust the influence topology of particles. According to studies on particle swarm optimization (PSO), which also examined the influence of its hyperparameters, the swarm can vary or converge too early due to improper values of inertia or learning coefficients [4]. These issues have led to the introduction of parallel PSO implementations that employ distributed evaluation of possible solutions. Particle swarm optimization (PSO) has been adapted to many-objective frameworks as the number of these objectives increases. According to Shu et al. [5], PSO works well in problems with a small number of objectives, but as dimensionality rises, its efficacy decreases.In order to overcome this constraint, hybrid approaches that integrate PSO with Pareto-ranking schemes or decomposition-based techniques have been put forth, enabling the algorithm to maintain both population diversity and convergence.

Differential Evolution (DE) has also shown reliable performance in CMOS optimization, especially when the design space is highly irregular, multimodal, and tightly constrained [6]. Zhao et al. [7] demonstrated DE's capability by combining it with a deterministic direct search for fully automated op-amp synthesis. In multi-objective contexts, advanced DE variants such as GDE3 have been employed in conjunction with surrogate models to reduce computational cost. Vişan et al. [8] demonstrated a Gaussian process-assisted GDE3 for optimizing a folded-cascode OTA, achieving wide Pareto front coverage with a significantly reduced number of SPICE simulations. Recently, DE has also been embedded within Bayesian Optimization frameworks to address budget-constrained optimization problems [9]. Cuckoo Search (CS), inspired by the brood parasitism behavior of certain cuckoo species and characterized by Lévy flight-based random walks, has emerged as a powerful alternative for analog sizing problems that demand both aggressive exploration and the ability to fine-tune within narrow feasible corridors.

The heavy-tailed step distribution inherent to Lévy flights enables CS to traverse wide regions of the design space, thereby avoiding premature convergence a common challenge in constrained analog design tasks. In ultra-low-voltage design, where transistor sizing is tightly constrained by near-threshold operation, Fortes et al. [10] applied a standard CS algorithm to the design of a 0.25 V bulk-driven Miller OTA in 130 nm CMOS. CS has also been adapted for parasitic-aware layout optimization, as demonstrated by Abouelyazid et al. [11]. Their modified CS incorporated placement-and-routing-aware performance estimation, enabling the optimizer to maintain post-layout performance metrics closely aligned with pre-layout targets. A broader methodological assessment by Abualigah et al. [12] underscored CS's suitability for highly nonconvex analog design problems, emphasizing its ability to balance exploration and exploitation dynamically without extensive parameter tuning.

This low-sensitivity to parameter configuration is particularly valuable in industrial CAD flows, where rapid algorithm deployment is often prioritized over prolonged parameter calibration. Z. Xu et al. [13] showed that deterministic multi-objective methods can equal or even outperform evolutionary approaches on smaller analog design tasks. Lberni et al. [14] employed deep neural network surrogates to model the nonlinear input–output mapping of analog circuits, embedding these models within the evolutionary loop. This approach reduced the reliance on computationally expensive SPICE evaluations while preserving high-fidelity optimization, enabling larger design spaces to be explored under fixed computational budgets. Complementary enhancements such as yield-aware optimization [15] and feasibility-biased initial population generation [16] have been increasingly incorporated into hybrid EA frameworks.

II.1 MAJOR GAPS IN THE LITERATURE:

- Evolutionary algorithms are effective for analog circuit sizing but struggle with many-objective problems, strict design constraints, and process variability.
- A scalable and unified optimization framework that addresses these challenges is still lacking.
- Current methods rely heavily on SPICE-in-the-loop evaluations and lack smooth integration into industrial CAD flows.
- There is a need for a holistic approach that unites evolutionary search, surrogate modeling, and deterministic refinement to enable practical, automation-ready analog circuit design.

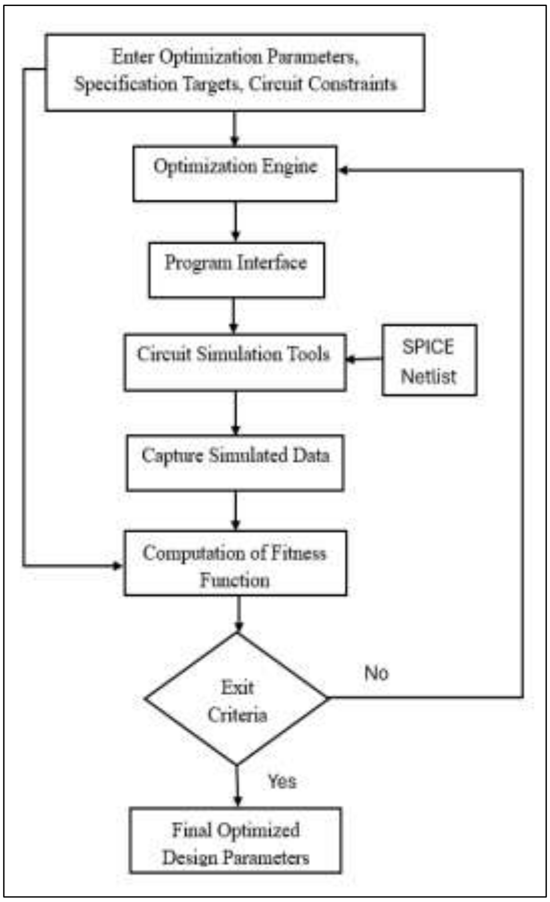

Figure 1: Adopted framework for automated circuit design methodology.
Source: Authors, (2026).

III. MATERIALS AND METHODS

The schematic representation of the automated CMOS analog circuit design framework, as depicted in Figure 1, constitutes a subset of a broader design automation environment. In this framework, the circuit topology is selected beforehand and treated as fixed. The system combines an evolutionary optimization engine with a SPICE-based simulator to synthesize CMOS analog circuits that meet defined performance targets. The optimizer systematically tunes transistor dimensions and bias conditions, while each candidate solution is validated through Ngspice simulations [17]. At every iteration, a parameterized SPICE netlist is generated to capture the electrical behavior of the design. MOS devices are constrained to operate in saturation, verified through bias point analysis and voltage transfer characteristics. The netlist is passed to the simulator to ensure device-level consistency, and a dedicated interface coordinates data flow between the optimizer and SPICE. Optimization begins with EA initialization, defining design variables, bounds, and objectives, followed by population generation and evaluation. This iterative co-simulation process enables detailed exploration of the design space and guides convergence toward high-fidelity solutions that satisfy analog performance requirements. Based on the outcomes produced by the circuit simulator, the fitness function of the circuit is quantitatively evaluated according to the following mathematical formulation [18].

$$Fitness\ Function = \sqrt{\sum_{j=1}^{D}\left(\frac{Specification_{desired} - Specification_{simulated}}{Specification_{desired}}\right)_j^2} \tag{1}$$

Here, D denotes the total number of targeted design specifications. This formulation essentially computes the Root Mean Square (RMS) error, thereby attributing equal weighting to all specifications, irrespective of their individual magnitudes or sensitivities. Consequently, the optimizer is compelled to satisfy each specification with comparable emphasis, ensuring a balanced trade-off among potentially conflicting performance objectives. Following the evaluation of the fitness function, the process proceeds to the termination check. The optimization cycle is concluded only if the pre-defined stopping conditions are fulfilled. In this work, the termination criteria are established as either (i) achieving a fitness function value below a stringent threshold of 1×10^{-6}, or (ii) reaching the upper bound of 100 iterations. Should neither condition be met, the evolutionary algorithm (EA) generates a new candidate set of design parameters, and the cycle is repeated.

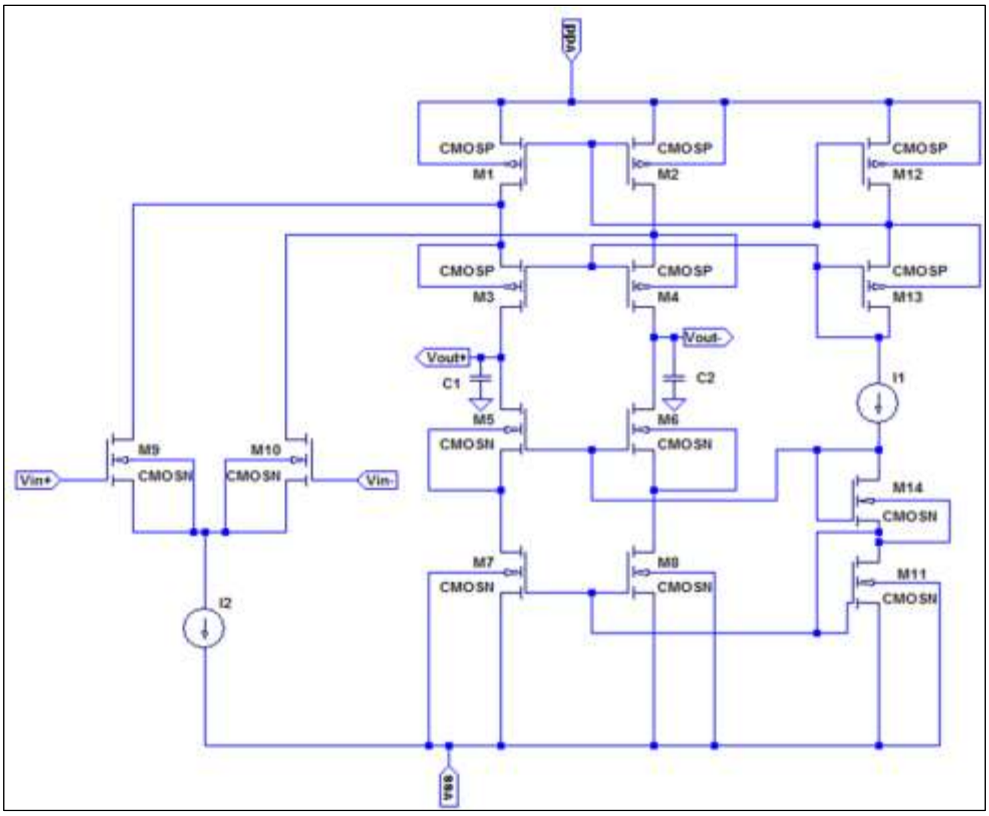

Figure 2: Folded Cascode OTA.
Source: Authors, (2026).

This iterative refinement embodies the optimizer's primary objective: to progressively reduce the fitness function value at each successive iteration until convergence to the desired solution is realized. The optimizer's performance depends on factors such as hyperparameter tuning, design space complexity, variable ranges, and the number of specifications to be met. This work applies three metaheuristic algorithms PSO, DE, and CS to optimize CMOS analog circuits, enabling a comparative assessment of their efficiency, robustness, and suitability for design automation.

IV. RESULTS AND DISCUSSIONS

The circuit diagram of CMOS Folded Cascode OTA (FOTA) is shown in Figure 2 [19]. More theoretical and mathematical analysis of this circuit can be found in [19], [20]. We have considered the width of M1, M2, and M12 transistors as W1 = W2 = W12, the width of M3 and M4 transistors as W3 = W4, the width of M5 and M6 transistors as W5 = W6, the width of M7 and M8 transistors as W7 = W8, the width of M9 and M10 transistors as W9 = W10, the width of M11 transistor as W11, the width of M13 transistor as W13, and the width of M14 transistors as W14 for this circuit. We have set the length of all transistors as L = 1 µm. So, this circuit has nine design parameters namely W1 = W2 = W12, W3 = W4, W5 = W6, W7 = W8, W9 = W10, W11, W13, W14, and I_{bias}. The circuit is optimized to drive the load capacitor of 0.1 pF. The supply voltage is set to ±1.8 V and ±2 V for both 0.18 µm and 0.35 µm CMOS technologies respectively.

Table 1: Search space and optimized parameters by different EAs for FOTA using 0.35 µm CMOS technology.

Sr. No.	Design Parameters	Search Space of Design Parameters	Optimized values of Design Parameters				
			PSO	DE	CS	[20]	[19]
1	$W_{1,2,12}$ (µm)	1 µm to 200 µm	196.24	200	121.31	25.6	28.5
2	$W_{3,4}$ (µm)	1 µm to 200 µm	94.6	93.77	35.11	12.8	49.9
3	$W_{5,6}$ (µm)	1 µm to 200 µm	163.95	200	143.37	4.5	16.4
4	$W_{7,8}$ (µm)	1 µm to 200 µm	163.95	200	143.37	4.5	34.2
5	$W_{9,10}$ (µm)	1 µm to 200 µm	195.34	200	164.99	49.2	49.85
6	W_{11} (µm)	1 µm to 200 µm	200	200	71.37	9	68.4
7	W_{13} (µm)	1 µm to 200 µm	200	200	100.21	25.6	99.8
8	W_{14} (µm)	1 µm to 200 µm	187.98	200	75.07	9	32.8
9	I_{bias} (µA)	1 µA to 200 µA	116.08	133.42	130.54	27.5	30

Source: Authors, (2026).

Table 2 presents a comparative summary of both the targeted specifications and the achieved simulated values corresponding to the optimized design parameters obtained through the application of different evolutionary algorithms (EAs) to this circuit. For this design case, a total of twelve distinct performance specifications are imposed, namely: open-loop voltage gain (Av), unity-gain bandwidth (UGB), phase margin (PM), positive power supply rejection ratio (+PSSR), negative power supply rejection ratio (–PSSR), rail-to-rail swing ratio (RSR), full swing ratio (FSR), common-mode rejection ratio (CMRR), power dissipation (P_{diss}), input-referred noise spectral density (Nin) at 10 kHz, integrated input-referred noise (N_{int}) across the frequency band from 1 Hz to 100 kHz, and the Total MOS Transistor Area (TTA).

The search space and optimized values achieved by different EAs for the design parameters of this circuit using 0.35 µm CMOS technology are found better than [19] and [20] listed in Table 1. Previous investigations have also explored the optimization of this circuit topology under comparable CMOS technologies. Vural et al. [21] reported the application of the standard Particle Swarm Optimization (PSO) algorithm for the design of this circuit, while Mallick et al. [22] extended this line of research by employing a Craziness-based PSO (CRPSO) variant to further enhance the exploration capabilities of the swarm and mitigate premature convergence issues. In comparison, the present results demonstrate improved performance over those reported by Vural et al. [21] using standard PSO and by Mallick et al. [22] with the CS variant, as summarized in Table 2.

Table 2: Desired specifications and obtained specifications by different EAs for FOTA using 0.35 µm CMOS technology.

Sr. No.	Specifications	Desired value	Obtained Specifications				
			PSO	DE	CS	[21]	[22]
1	A_V (dB)	> 70	74.15	73.53	74.45	76	85. 5
2	UGB (MHz)	> 100	157.70	156.39	219.42	420	537
3	PM (°)	> 45	83.64	64.97	81.79	--	---
4	+ve PSSR (dB)	> 65	68.82	68.93	70.03	57.68	79
5	- ve PSSR (dB)	> 75	84.85	85.16	83.24	57.68	79
6	RSR (V/µs)	> 40	155.89	90.40	85.49	200	290
7	FSR (V/µs)	> 40	53.83	54.33	67.85	200	290
8	CMRR (dB)	> 80	117.50	129.88	110.97	59.23	61.75
9	P_{diss} (mw)	< 1	0.739	0.851	0.880	0.66	0.696
10	N_{in} (nV^2/Hz)	< 1e-6	7.75 e-8	6.75 e-8	5.23 e-8	--	---
11	N_{op} (nV^2/Hz)	< 1e-3	4.06 e-4	3.44 e-4	4.26 e-4	--	---
12	TTA (µm^2)	< 3000	2412.38	2587.54	1584.26	262.4	1155.37

Source: Authors, (2026).

Table 3: Performance of different EAs for optimization of FOTA using 0.35 µm CMOS technology.

Algorithm	$SD_{fitness}$	$Iter_{avg}$	FE_{avg}	S_{rate}	T_{sim} (s)
DE	**0.030888**	60	1857	8	3835
PSO	0.233654	56.40	**1692**	5	**3393**
CS	0.090025	56.20	3402	**9**	6442

Source: Authors, (2026).

The desired design specifications, along with the corresponding values obtained through parameter optimization using different evolutionary algorithms (EAs) for this circuit in a 0.35 µm CMOS technology, are summarized in Table 1. The comparative performance of three well-established optimization techniques PSO, DE and CS was systematically evaluated through 10 independent experimental runs, as presented in Table 3. The CS algorithm showed the greatest robustness, meeting all target specifications in 9 of 10 runs, compared with eight for DE and five for PSO. These results position CS as a promising tool for complex analog design tasks involving high-dimensional parameter spaces and tight performance constraints. For the 0.18 µm CMOS implementation, Table 4 lists the parameter search ranges alongside the optimized values obtained by each algorithm. The results highlight the efficiency with which different algorithms navigate the high-dimensional search landscape to satisfy stringent performance specifications.

The desired design specifications are presented in Table 5 for the circuit implemented in 0.18 µm CMOS technology. A detailed performance comparison of PSO, DE, and CS across 10 independent optimization trials is provided in Table 6. The results reveal that both CS and DE consistently achieved convergence to all targeted specifications in every run. PSO achieved full specification compliance in only 4 of 10 runs, reflecting weaker robustness in navigating the circuit's design space. Evaluation of CS showed the most efficient convergence, requiring fewer iterations on average than both DE and PSO. This efficiency reflects CS's stronger balance between exploration and exploitation in high-dimensional spaces. While DE demanded slightly more computation than CS, it remained more reliable and efficient than PSO.

Table **Erro! Nenhum texto com o estilo especificado foi encontrado no documento.**: Search space and optimized parameters by different EAs for FOTA using 0.18 µm CMOS technology.

Sr. No.	Design Parameters	Search Space of Design Parameters	Optimized values of Design Parameters		
			PSO	DE	CS
1	$W_{1,2,12}$ (µm)	1 µm to 200 µm	110.47	200	44.81
2	$W_{3,4}$ (µm)	1 µm to 200 µm	99.66	74.85	3.79
3	$W_{5,6}$ (µm)	1 µm to 200 µm	172.18	200	174.84
4	$W_{7,8}$ (µm)	1 µm to 200 µm	172.18	200	174.84
5	$W_{9,10}$ (µm)	1 µm to 200 µm	108.2	200	63.72
6	W_{11} (µm)	1 µm to 200 µm	200	149.89	7.44
7	W_{13} (µm)	1 µm to 200 µm	159.5	200	181.08
8	W_{14} (µm)	1 µm to 200 µm	175.58	200	96.17
11	I_{bias} (µA)	1 µA to 200 µA	142.84	130.32	149.55

Source: Authors, (2026).

Table 5: Desired specifications and obtained specifications by different EAs for FOTA using 0.18 µm CMOS technology.

Sr. No.	Specifications	Desired value	Obtained Specifications		
			PSO	DE	CS
1	A_V (dB)	> 70	77.71	77.86	79.03
2	UGB (MHz)	> 100	167.19	146.54	194.02
3	PM (°)	> 45	76.72	70.13	80.93
4	+ve PSSR (dB)	> 65	77.92	77.09	78.47
5	- ve PSSR (dB)	> 75	77.35	78.55	79.67
6	RSR (V/µs)	> 10	88.09	166.63	40.43
7	FSR (V/µs)	> 10	52.95	41.01	57.69
8	CMRR (dB)	> 80	137.17	139.92	140.35
9	P_{diss} (mw)	< 1	0.867	0.779	0.843
10	N_{in} (nV^2/Hz)	1e-6	4.06 e-8	5.11 e-8	2.51 e-8
11	N_{op} (nV^2/Hz)	1e-3	2.79 e-4	2.96 e-4	2.77 e-4
12	TTA ($µm^2$)	< 3000	1970.93	2499.59	1253.5

Source: Authors, (2026).

Table 6: Performance of different EAs for the optimization of FOTA using 0.18 µm CMOS technology.

Algorithm	$SD_{fitness}$	$Iter_{avg}$	FE_{avg}	S_{rate}	T_{sim} (s)
DE	0.0	38	1170	10	2428
PSO	0.218294	69	2067	4	4088
CS	0.0	38.30	2328	10	4493

Source: Authors, (2026).

Taken together, these findings establish that while both CS and DE demonstrate strong potential as optimization frameworks for analog circuit design in deep-submicron CMOS technologies, CS holds a distinctive advantage due to its consistent reliability coupled with faster convergence. The weaker performance of PSO in this study highlights the shortcomings of swarm-based heuristics when applied to highly constrained, nonlinear, and multi-objective design problems. By comparison, the results point to CS and DE as more effective optimization strategies for analog design automation at the 0.18 µm technology node.

V. CONCLUSIONS

This work examined the use of the Cuckoo Search (CS) algorithm for automated design of CMOS analog circuits, focusing on the Folded Cascode OTA in 0.18 µm and 0.35 µm technologies. When compared to Particle Swarm Optimization (PSO) and Differential Evolution (DE), CS consistently produced higher success rates, faster convergence, and more robustness under demanding design constraints. In 9 of 10 trials, CS converged for the 0.35 µm process, surpassing DE with 8 and PSO with 5. The effectiveness of CS across technology scales is confirmed by similar results at 0.18 µm.The study emphasizes DE's relative competitiveness while highlighting PSO's shortcomings in complex analogue design. However, CS was able to strike an improved balance between exploration and improvement, which made it a dependable method for circuit automation in the face of complexity and scaling issues. Because of its proven effectiveness, it can be integrated into next-generation CAD platforms for mixed-signal SoCs, which can shorten development cycles and increase design productivity. Future directions include extension to advanced nodes, multi-objective strategies that explicitly recognize trade-offs in power, area, and noise, and hybrid approaches that integrate CS with other heuristics.

VI. AUTHOR'S CONTRIBUTION

Conceptualization: Pankaj P. Prajapati, Alpesh M. Patel, Kirit V. Patel, and Ghanshyamkumar Sah.
Methodology: Pankaj P. Prajapati, Anilkumar J. Kshatriya, Kirit V. Patel, and Kinjal R. Sheth.
Investigation: Pankaj P. Prajapati, Alpesh M. Patel, Chintan Dave, and Devendra H. Patel.
Discussion of results: Anilkumar J. Kshatriya, Alpesh M. Patel, Kirit V. Patel, and Devendra H. Patel.
Writing – Original Draft: Pankaj P. Prajapati, Alpesh M. Patel, Ghanshyamkumar Sah, and Anilkumar J. Kshatriya.
Writing – Review and Editing: Alpesh M. Patel, Anilkumar J. Kshatriya, Kinjal R. Sheth and Ghanshyamkumar Sah.
Resources: Pankaj P. Prajapati, Kirit V. Patel, Chintan Dave, Devendra H. Patel and Kinjal R. Sheth.
Supervision: Pankaj P. Prajapati, Ghanshyamkumar Sah, Chintan Dave and Devendra H. Patel.
Approval of the final text: Alpesh M. Patel, Pankaj P. Prajapati, Chintan Dave, and Kinjal R. Sheth.

VII. REFERENCES

[1] K. G. Shreeharsha, R. K. Siddharth, M. H. Vasantha and Y. B. N. Kumar, "Partition Bound Random Number-Based Particle Swarm Optimization for Analog Circuit Sizing," in IEEE Access, vol. 11, pp. 123577-123588, 2023, doi: 10.1109/ACCESS.2023.3329698

[2] W. Liu, Z. Wang, N. Zeng, Y. Yuan, F. E. Alsaadi, and X. Liu., "A novel randomised particle swarm optimizer," International Journal of Machine Learning and Cybernetics, vol. 12, no. 2, pp. 529–540, 2021, doi: 10.1007/s13042-020-01186-4.

[3] H. Bouali, B. Benhala, and M. Guerbaoui, "Multi-objective optimization of CMOS low noise amplifier through nature-inspired swarm intelligence," Bulletin of Electrical Engineering and Informatics, vol. 12, no. 5, pp. 2824–2836, Oct. 2023, doi: 10.11591/eei.v12i5.5512.

[4] H. Xu, Q. Deng, Z. Zhang, and S. Lin, "A hybrid differential evolution particle swarm optimization algorithm based on dynamic strategies," Scientific Reports, vol. 15, Art. no. 4518, Feb. 2025, doi: 10.1038/s41598-024-82648-5.

[5] X. Shu, Y. Liu, and Q. Zhang, "A novel multiobjective particle swarm optimization combining hypercube and distance," Scientific Programming, vol. 2022, Art. ID 9448419, 2022, doi: 10.1155/2022/9448419.

[6] D. Joshi, S. Dash, S. Reddy, R. Manigilla, and G. Trivedi, "Multi-objective hybrid particle swarm optimization and its application to analog and RF circuit optimization," Circuits, Systems, and Signal Processing, vol. 42, no. 8, pp. 4443–4469, 2023, doi: 10.1007/s00034-023-02342-1.

[7] Z. Zhao, J. Liu, and L. Zhang, "Acceleration for efficient automated generation of operational amplifiers," Sensors (Basel), vol. 24, no. 12, art. no. 3990, 20 Jun. 2024, doi: 10.3390/s24123990.

[8] C. Vişan, O. Pascu, M. Stănescu, E.-D. Şandru, C. Diaconu, A. Buzo, G. Pelz, and H. Cucu, "Automated circuit sizing with multi-objective optimization based on differential evolution and Bayesian inference," Knowledge-Based Systems, vol. 258, p. 109987, 2022, doi: 10.1016/j.knosys.2022.109987.

[9] L. Kouhalvandi, O. Ceylan, and S. Ozoguz, "Optimization techniques for analog and RF circuit designs: An overview," Analog Integrated Circuits and Signal Processing, vol. 106, no. 3, pp. 511–524, 2021, doi: 10.1007/s10470-020-01733-7.

[10] A. Fortes, F. A. Quirino, L. A. da Silva, and A. Girardi, "Low power bulk-driven OTA design optimization using cuckoo search algorithm," Analog Integrated Circuits and Signal Processing, vol. 106, no. 1, pp. 99–109, 2020, doi: 10.1007/s10470-020-01632-x.

[11] M. S. Abouelyazid, S. Hammouda, and Y. Ismail, "RC parasitic-aware layout analysis and routing optimization methodology," IEEE Access, vol. 10, pp. 92740–92759, 2022, doi: 10.1109/ACCESS.2022.3203077.

[12] L. Abualigah, A. Ababneh, A. M. Ikotun, R. Abu Zitar, A. R. Alsoud, N. Khodadadi, A. E. Ezugwu, E. S. Hanandeh, and H. Jia, "A survey of cuckoo search algorithm: optimizer and new applications," in Metaheuristic Optimization Algorithms, Elsevier, 2024, pp. 45–57, doi: 10.1016/B978-0-443-13925-3.00018-2.

[13] Z. Xu, Z. Zhao, and J. Liu, "Deterministic multi-objective optimization of analog circuits," Electronics, vol. 13, no. 13, p. 2510, 2024, doi: 10.3390/electronics13132510.

[14] A. Lberni, M. A. Marktani, A. Ahaitouf, and A. Ahaitouf, "Analog circuit sizing based on evolutionary algorithms and deep learning," Expert Syst. Appl., vol. 237, art. no. 121480, Mar. 2024, doi: 10.1016/j.eswa.2023.121480.

[15] A. Canelas, F. Passos, N. Lourenço, R. Martins, E. Roca, R. Castro-Lopez, N. Horta, and F. V. Fernández, "Hierarchical yield-aware synthesis methodology covering device-, circuit-, and system-level for radiofrequency ICs," IEEE Access, vol. 9, pp. 124152–124164, 2021, doi: 10.1109/ACCESS.2021.3110758.

[16] M. Zuo and Y. Xue, "Population feasibility state guided autonomous constrained multi-objective evolutionary optimization," Mathematics, vol. 12, no. 6, art. no. 913, Mar. 2024, doi: 10.3390/math12060913.

[17] P. Nenzi and H. Vogt, Ngspice User's Manual. 2014. [Online]. Available: http://ngspice.sourceforge.net/

[18] Fakhfakh, M., Cooren, Y., Sallem, A., Loulou, M., & Siarry, P., "Analog Circuit Design Optimization through the Particle Swarm Optimization Technique," Analog Integrated Circuits and Signal Processing, vol. 63, no. 1, pp. 71–82, Jan. 2010. doi: 10.1007/s10470-009-9361-3.

[19] A. Kaur and M. Kaur, "A comprehensive survey of test functions for evaluating the performance of particle swarm optimization algorithm," Int. J. Hybrid Inf. Technol., vol. 8, no. 5, pp. 97–104, 2015. doi: 10.14257/ijhit.2015.8.5.10.

[20] M. M. Ali and A. Törn, "Population set-based global optimization algorithms: Some modifications and numerical studies," Comput. Oper. Res., vol. 31, no. 10, pp. 1703–1725, 2004. doi: 10.1016/S0305-0548(03)00116-3.

[21] R. A. Vural and T. Yildirim, "Analog circuit sizing via swarm intelligence," Int. J. Electron. Commun., vol. 66, no. 9, pp. 732–740, 2012

[22] S. Mallick, R. Kar, S. P. Ghoshal, and D. Mandal, “Optimal sizing and design of CMOS analogue amplifier circuits using craziness-based particle swarm optimization,” Int. J. Numer. Model. Electron. networks, devices fields, vol. 29, no. 5, pp. 943–966, 2016. doi: 10.1002/jnm.2155. ;