Journal of Engineering and Technology for Industrial Applications

ISSN ONLINE: 2447-0228

ITEGAM-JETIA

Manaus, v.11 n.56, p.257-266. November/December, 2025.
DOI: https://doi.org/10.5935/jetia. v11i56.2751

RESEARCH ARTICLE OPEN ACCESS

NEW RECONFIGURABLE IMPLEMENTATION OF PARALLEL INTRA PREDICTION ALGORITHM IN VIRSATILE VIDEO CODING

Wahiba Menasri[1], Abderrezak Gacemi[2], Abdelhalim Tlemçani*[3]

[1,2]Energies and Materials Electronics departement University of Medea, Medea, Algeria.
[3]Electrical Engineering and Automation Research Laboratory (LREA), University of Medea, Medea, Algeria.

[1]http://orcid.org/ 0009-0005-5458-4173, [2]https://orcid.org/0009-0001-8333-7519, [3]http://orcid.org/ 0000-0002-4385-671X

Email: menasri.wahiba@univ-medea.dz, gacemi.abderrezak@univ-medea.dz, tlemcani.abdelhalim@univ-medea.dz

ARTICLE INFO

Article History
Received: September 27, 2025
Revised: November 20, 2025
Accepted: December 1, 2025
Published: December 31, 2025

Keywords:
Versatile Video Coding,
FPGA implementation,
Linear Model Prediction,
Parallel architecture,
VVC intra prediction.

ABSTRACT

Versatile Video Coding (VVC/H.266) introduces significantly enhanced intra prediction technique compared to its predecessors, leading to notable compression efficiency gains, especially for high-resolution and screen content. However, these improvements come at the price of more complexity implementation. VVC intra prediction modes are planar, Direct Component (DC), angular and a novel one Cross-Component Linear Model Prediction (CCLM). This paper presents a novel parallel architecture and an effective FPGA-based implementation of intra prediction algorithm in VVC codec. The intra prediction modes are designed and implemented separately on hardware and software environments in order to validate our proposed solution. After that, full intra prediction design is presented by combining four previously modes and by introducing parallel technique. The improvements of our work are given on three levels, firstly, our FPGA parallel intra prediction implementation can process 6 samples and operate with a good frequency value of 178 Mhz (throughput of 1068 samples/s) with acceptable number of resources in terms of 12000 LUTs. Secondly, the obtained area efficiency is about 0.089 samples/s/ LUTs which is better to that given in literature for VVC intra prediction algorithm. Finally, this work is the only which presents full FPGA implementation of VVC intra prediction.

I. INTRODUCTION

The H.266/VVC standard is a new and latest video coding technology, which is finalized on 6 July 2020. VVC is developed by the Joint Video Experts Team (JVET) of the International Standardization Organization (ISO/IEC) Moving Picture Experts Group (MPEG) and International Telecommunication Union (ITU-T) Video Coding Experts Group (VCEG) to improve compression efficiency compared with its predecessor HEVC and AVC [1-3]. At the same video quality, especially for Ultra High Definition (UHD) video, the VVC standard currently provides between 25 and 30\% Bitrate saving compared to its predecessor H.265/HEVC [1], [2] but at the cost of increased algorithm complexity. Indeed, VVC is constructed by a modified and improved of many techniques used in HEVC, such as multiple reference frames, Transform Block (TB) sizes, and intra prediction, inter prediction, Sample Adaptive Offset (SAO) and deblocking filter, and CABAC entropy coding [2].

In addition, VVC also introduces a new method aimed at further improving throughput while maintaining the same quality of the processed information such as the new in-loop filtering technologies: Adaptive Loop Filtering (ALF), Cross-Component Adaptive Loop Filtering (CC-ALF) and Luma Mapping with Chroma Scaling (LMCS),.Etc. One of the basic tools used in video codec is the Intra prediction technique. It plays a crucial role in reducing the redundancy within video Intra frames, which result a positive impact on the efficient of video compression. Intra prediction operates on a pixel level within a video picture, predicting the values of pixels based on the neighboring pixels of the same picture. So, it exploits the spatial redundancy present in natural video content by using previously encoded samples to estimate the values of pixels in the current block being encoded [3]. The VVC intra prediction algorithm is modified compared to that adopted in HEVC by extending the number of prediction modes and improved each of them in order to enhance the prediction efficiency and increase the coding/decoding throughput but at the cost of hard computational complexity. The tools used in intra VVC are the following: firstly, planar and DC interfacial modes which operate with the same principle of operation [4]. Secondly, extended number of angular intra prediction mode TO 65 instead of 32 modes used in the previous video codec HEVC, to estimate pixel values within blocks [1], [5]. Thirdly, the important and the new intra prediction modes in VVC is the Cross-Component Linear Model (CCLM) which eliminate the linear correlation between the luma and chroma components in a coding block [2]. The CCLM mode may be split into three (03) modes according to whether left samples, upper samples or both thereof and may apply only to a chroma component: L_CCLM, T_CCLM and LT_CCLM [6]. This new mode CCLM improves the efficiency of intra prediction which affects directly the overall throughput of the encoding and decoding VVC processes but at the expense of an increase in implementation complexity.

Several works of intra prediction algorithm in the two previous standards AVC and HEVC are proposed in literature based on software and/or hardware implementations, but a few of them are based on the intra prediction in VVC standard. Additionally, little designs are being carried out to the study and hardware implementation with optimized intra prediction algorithm which affect directly the overall throughput of VVC decoding process. Study of intra prediction technique in the latest video coding standard VVC is given in [7]. So, all prediction modes are presented as well as: 65 angular intra prediction modes, DC mode, planar mode and the new mode CCLM. Low-complexity refinements of HEVC intra prediction is proposed in [8] and are applied on the three modes planar, DC and angular mode. The experimental results obtained by JEM-7.0 achieved an average of 0.7\% of coding gain with the same run-time complexity. How is designed an efficient software implementation of the Matrix-Based Intra Prediction modes is presented in [9] based on two techniques: the geometrically transforming technique and a soft-clipping function to improve the integer quantization and to restrict the range of floating-point matrix entries.

The all-Intra bit-rate is savings of 0.6\% across different resolutions. In paper [10], an efficient Field Programmable Gate Array (FPGA) partial implementation of HEVC intra prediction is proposed for 4x4, 8x8, 16x16 and 32x32 angular prediction modes which can process 55 Full HD (1920x1080) frames per second and it has up to 34.66\% less energy consumption than the conventional FPGA implementation of HEVC intra prediction. An efficient FPGA implementation of partial VVC intra prediction algorithm (angular modes) is proposed in [11] for the following prediction unit sizes: 4x4, 8x8, 16x16 and 32x32 pixels. This design can process 34 full HD (1920x1080) frames per second in the worst case. A novel technique is proposed in [12] to reduce the number of computations and energy consumption of angular modes intra prediction algorithm in HEVC codec. This work is designed, implemented using Verilog HDL and applied only for luminance prediction units. The first FPGA implementation proposed in literature of HEVC intra prediction using an HLS tool is given [13].

The proposed design, can process 35 full HD (1920x1080) video frames per second in the worst case. Performance evaluation between two implementation methods software (Central Processor Unit (CPU)) and software/hardware (CPU/FPGA) of intra prediction in terms of area cost, run time and power consumption is implemented in [14]. The obtained results show that the mixed method software/hardware is faster than software implementation with 50\% in term of run time and the power consumption is saved by 80\% approximately. A new optimized implementation of angular modes intra prediction for 4×4 prediction unit is proposed in [15]. This architecture is synthesized with two technologies. The Complementary Metal-Oxide-Semiconductor (CMOS) technology which consume 15010 logic gates and operate at 218 Mhz. The FPGA (Xilinx Virtex 6) technology with 234 MHZ of frequency and consume 1654 Look Up Tables (LUTS).

An efficient VVC chroma intra prediction is proposed in [16], in which the colorization relationship between reference luma and chroma components is exploited to predict the chroma components for the current luma component but it is also partial solution. Multi-samples are predicted in [17-21] with 16, 8 and 8 samples respectively with full FPGA architecture but the solutions are given for HEVC codec. The works [8], [11] and [12] presented FPGA partial intra prediction algorithm (only angular mode) improved the energy consumption, complexity, number of computations, evaluate the performance between software and hardware implementation, …. etc. Otherwise, none of them proposed full FPGA intra prediction implementation with all-prediction modes supported with HEVC and VVC. In this work, we propose Parallel FPGA implementation of full intra prediction modes in the latest video codec VVC.

All prediction modes are implemented Planar, DC, angular modes and the new adopted mode CCLM. After that, these modes are combining to design the multi-samples architecture of VVC intra prediction based on the parallelism of the following stages: 2 parallel DC, 2 parallel planar, 2 parallel angular, and one CCLM modes. This proposed architecture can process multi predicted samples with good area efficiency. Moreover, our work is the only in literature which proposes FPGA implementation of full VVC intra prediction algorithm with four prediction modes. The rest of the paper is structured as follows: In section 2, the VVC intra prediction algorithm is presented. Section 3 is reserved to our proposed design of parallel intra prediction in the four modes adopted in VVC standard followed by the synthesized, validation and comparison results of our work in section 4. Finally, conclusion and perspectives are shown in Section 5.

II. VVC INTRA PREDICTION ALGORITHM

Different tools are called in VVC intra prediction such as: angular intra prediction with 65 angles, Wide-Angle Intra Prediction (WAIP), Matrix-based Intra Prediction (MIP), Multiple Reference Line (MRL) prediction, etc. Meanwhile, VVC intra prediction is based on four modes, where the three modes DC, Planar, 65 intra-angle modes are the same modes called in its predecessor HEVC with extended number of angular direction modes from 33 to 65 (as shown in Fig.1) and the fourth one is new adopted in VVC, CCLM mode which is sub-divided into 3 CCLM modes. For example, the intra prediction mode be indexed as shown in Table 1 below.

II.1 DC MODE INTRA PREDICTION

In this mode, the predicted samples (PredSamples) are obtained by using the following three equations and depends on the size of the current block to be processed and the position of samples in within the block. The predicted block size can be equal to: 4 x 4, 8 x

8, 16 x 16, 32 x 32 and 64 x 64. One of the three equations (Eq1, Eq2 and Eq3) is selected to get the PredSamples in this mode which is equal to DC value (ValDC). The (x, y) variables can be ranging between the following values (x = 0..nTbW \– 1, y = 0..nTbH \– 1).

$$\text{ValDC} = \left(\sum_{x'}^{nTbW-1} p[x'][-1-\text{refIdx}] + \sum_{y'}^{nTbH-1} p[-1-\text{refIdx}][y'] + nTbW \right) >> \left(\text{Log2}(nTbW) + 1 \right) \quad (1)$$

$$\text{ValDC} = \left(\sum_{x'}^{nTbW-1} p[x'][-1-\text{refIdx}] + (nTbW >> 1) \right) >> \text{Log2}(nTbW) \quad (2)$$

$$\text{ValDC} = \sum_{y'}^{nTbH-1} p[-1-\text{refIdx}][y'] + (nTbH >> 1) >> \text{Log2}(nTbH) \quad (3)$$

Table 1: VVC Intra prediction modes.

Intra prediction mode	Associated name
0	INTRA_PLANAR
1	INTRA_DC
2.66	INTRA_ANGULAR2..INTRA_ANGULAR66
81.83	INTRA_LT_CCLM, INTRA_L_CCLM, INTRA_T_CCLM

Source: Authors, (2025).

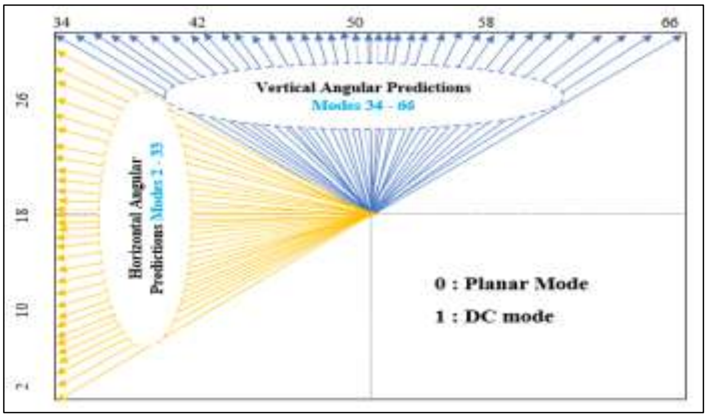

Figure 1: Angular directions, planar and DC Intra prediction modes in VVC standard.

Source: Authors, (2025).

II.2 PLANAR MODE INTRA PREDICTION

In the VVC Planar mode adopted, the predicted samples are obtained as a weighted average of 4 reference samples values. Here, the reference samples in the same row or column as the current sample and the reference samples on the bottom-left and on the top-right position with respect to the block are used [7]. According to the standard \cite{b4}, the planar mode is called for all prediction blocks sizes. At the picture level, this mode is perfect and applied for the image that does not result any discontinuities and does not contain edge model. In order to get the PredSamples in planar mode we use the equation Equ.6, which is based on the two following signal variables: Horizontal PredH[x][y] and Vertical PredV[x][y] obtained using the Equ.4 and Equ.5 respectively. The x and y position are ranging between 0 and (nTbH×nTbW-1).

$$\text{predH}[x][y] = ((nTbW - 1 - x) \times p[-1][y] + (x + 1) \times p[nTbW][-1]) << \text{Log2}(nTbH) \quad (4)$$

$$\text{predV}[x][y] = ((nTbH - 1 - y) \times p[x][-1] + (y + 1) \times p[-1][nTbH]) << \text{Log2}(nTbW) \quad (5)$$

$$\text{predSamples}[x][y] = (\text{predV}[x][y] + \text{predH}[x][y] + nTbW * nTbH) >> (\text{Log2}(nTbW) + \text{Log2}(nTbH) + 1) \quad (6)$$

II.3 ANGULAR MODE INTRA PREDICTION

In VVC standard, the number of directional modes available for a block to be processed is about 65 directions as given in Figure.1. Each direction has a specifique indices ranging from 2 to 66 and divided into two types according to the directions:

- ✓ Horizontal angular prediction modes (2 to 33 Directions);
- ✓ Vertical angular prediction modes (34 to 66 Directions).

The number of modes distribution depends on the type of partitioning prediction block:

- ✓ For blocks of square shape, an equal number of angular modes is assigned to the top and left side of a block;
- ✓ For intra blocks of rectangular shape, more intra prediction directions are assigned to the longer side of a block.

II.4 CCLM MODE INTRA PREDICTION

VVC intra prediction includes a new prediction mode CCLM in order to improve the coding/decoding efficiency by exploiting and predicting the redundant information of chroma samples from corresponding reconstructed luma samples. Moreover, the CCLM mode is assumed that the chromaticity pixel of the same coding block is linear with the corresponding luma pixel value [18]. Fig.2 presents the pixel values that need to be used in the calculation process, the prediction is carried out using a linear function (with a and b parameters) in the form equation (Equ.7):

$$P\ (i,j)=a\times re\acute{c}_L(I,j) \quad (7)$$

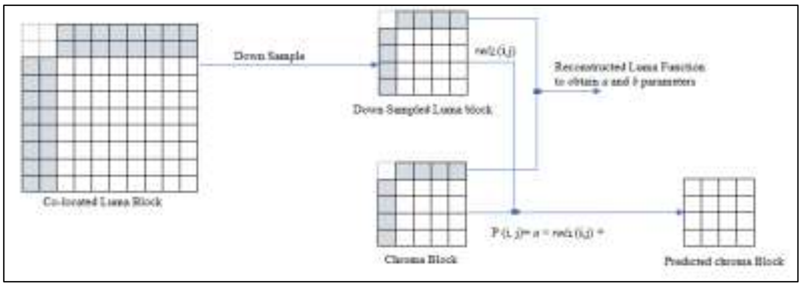

Figure 2: CCLM intra prediction mode process in VVC Standard.
Source: Authors, (2025).

With P(i; j) : the predicted chroma samples in a CU. rećL: Reconstructed luma samples of the same CU which are down sampled for the case of non- 4:4:4 color format. a and b: Linear parameters.
The intra prediction mode include CCLM mode for chroma samples in addition to the above-described intra prediction modes. This mode is divided into three sub-modes namely:

- ✓ L_CCLM (Left Cross Component Linear Model): the prediction is applied according to the left samples);
- ✓ T_CCLM (Top Cross Component Linear Model): the prediction is applied according to the top samples);
- ✓ LT_CCLM (Left Top Cross Component Linear Model): the prediction is applied according to the left and top samples).

One of three sub-modes is activated according to the following conditions:

- ✓ T_CCLM intra mode is activated when predModeIntra = INTRA T CCLM;
- ✓ L_CCLM intra mode is activated when predModeIntra = INTRA L CCLM;
- ✓ LT_CCLM intra mode is activated when predModeIntra = INTRA LT CCLM.

III. ROPOSED DESIGN OF VVC PARALLEL INTRA PREDICTION ALGORITHM

Our proposed block diagram of VVC intra prediction algorithm is shown in Figure 3 which is constructed by: two DC, two Planar, and two Angular and CCLM stages. This design is based on functional blocks where each block performs a specific task. According to the VVC standard, each mode is responsible to predict the PredSamples from the reconstructed and referenced ones. The novelty of the proposed hardware architecture is to increase the throughput of prediction with maintain acceptable number of resouces. Additionally, some techniques are adopted in this work in order to increase the peak of prediction to 6 samples per cycle such as:

- ✓ The rearrangement of memory (decrease the number of Block of Read Only Memory (BRAMs)) which is based on the storage of the data called at the same time in the same memory;
- ✓ Parallel technique is adopted between and within four modes stages.

As shown in figure 3, all stages called in the parallel architecture of VVC intra prediction will be detailled in the following sub-sections:

III.1 PROPOSED DESIGN OF DC PREDICTION MODE

The following Figure 4 shows our proposed design of DC mode in VVC intra prediction. At the input, different variables and fixed values are used to obtain the PredSamples. The inputs variables of this mode and their meanings are:

- ✓ nTbW: transform block width;
- ✓ nTbH: transform block height;
- ✓ refIdx specifying the intra prediction reference line index.

III.2 PROPOSED DESIGN OF PLANAR PREDICTION MODE

Figure 5 represents the calculation of predsamples using a set of variables and fixed values, specified by VVC standard. The Inputs variables of this architecture and their meanings are the following: nTbW, nTbH, and (x,y): position of current pixel.

III.3 PROPOSED DESIGN OF ANGULAR PREDICTION MODE

The predsamples in this mode are obtained as it is depicted in Figure 6 and Figure 7 respectively. The proposed design is divided into two parts (Angular part1 and Angular part2) to present better this algorithm and to give more details. The predicted angular samples horizontal or vertical is obtained by using a set of variables and fixed values: cIdx: Color component Index for current block, RefIdx: Intra Reference Line Index; predModeIntra: intra prediction mode, nTbW: transform block width, nTbH: transform block height, refW: reference samples width, refH: reference samples height, nCbH: coding block height, nCbW: coding block width, refFilterFlag: reference filter flag, P[x][y]: neighbouring samples. In order to get the predsamples, the output (character “A” in a closed yellow circuit) of Angular part1 given in Figure 6, s used as input for Angular part2 presented in Figure 7. The parallel and pipeline techniques are adopted to reduce the path delay and increase the number of predicted samples.

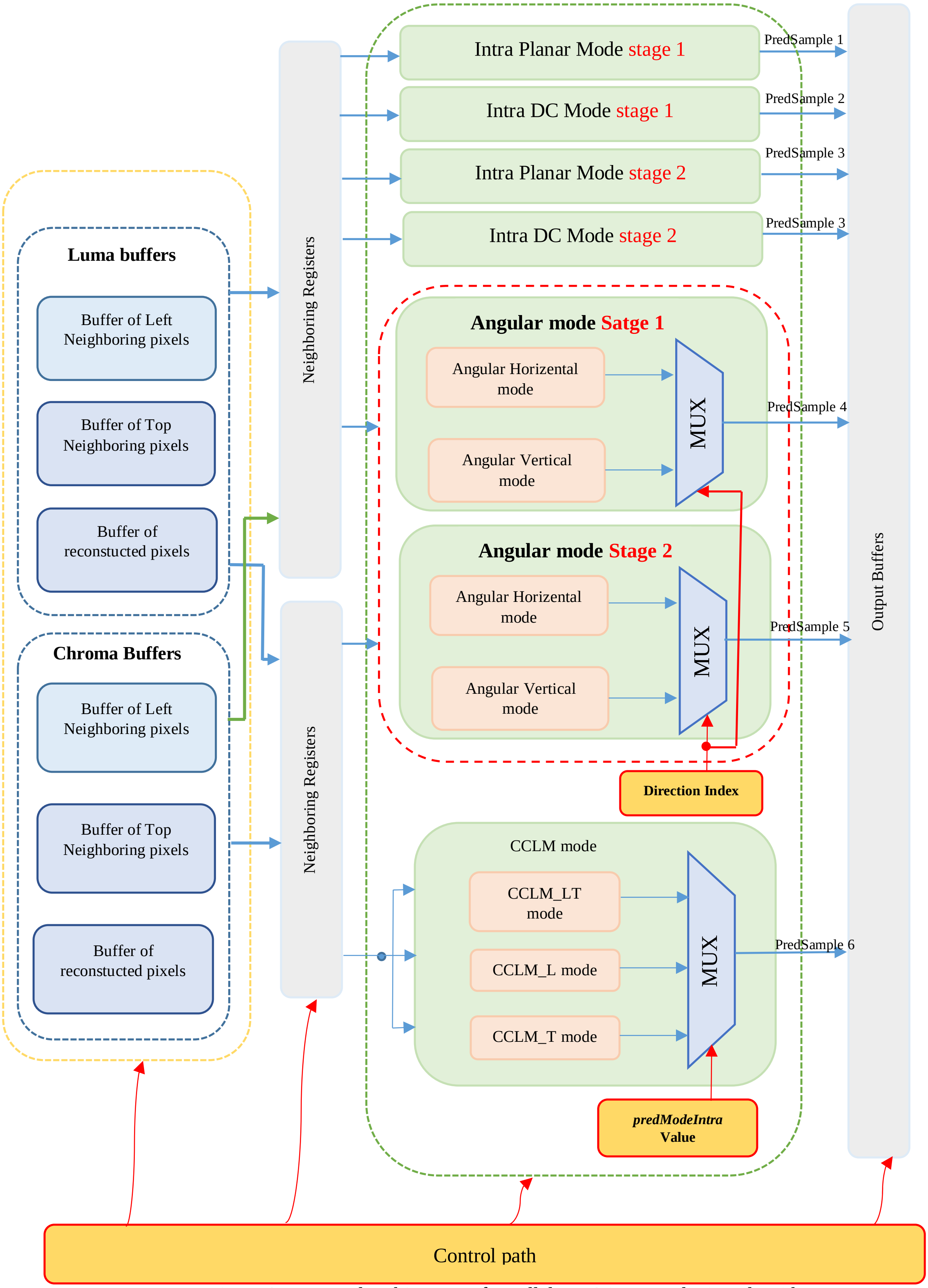

Figure 3: Proposed architecture of parallel VVC intra prediction algorithm.
Source: Authors, (2025).

III.4 PROPOSED DESIGN OF CCLM PREDICTION MODE

In this mode, the predsamples are obtained by using our proposed design which is also divided into two parts (CCLM part1 and CCLM part2) and presented in Figure 8 and Figure 9 respectively. Inputs to this process are: cIdx: Color component Index for current block, predModeIntra, nTbW, nTbH, (xTby,yTby): Luma location of top-left sample of current transform block, P[x][y] : neighboring samples. The output of CCLM part1 in Figure 8 (character "A" in a closed yellow circuit) is one of inputs of CCLM part2 Figure 9 in order to get the predsamples.

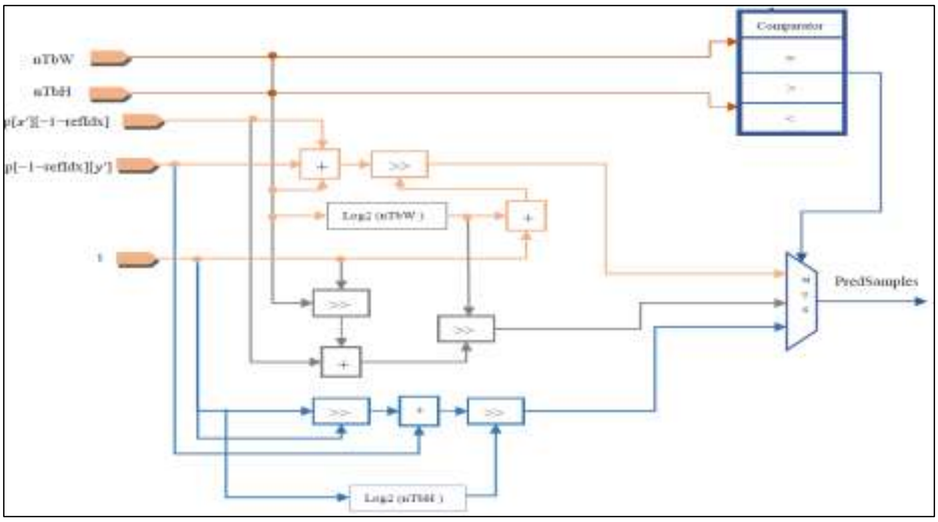

Figure 4: Proposed architecture of DC VVC intra prediction.
Source: Authors, (2025).

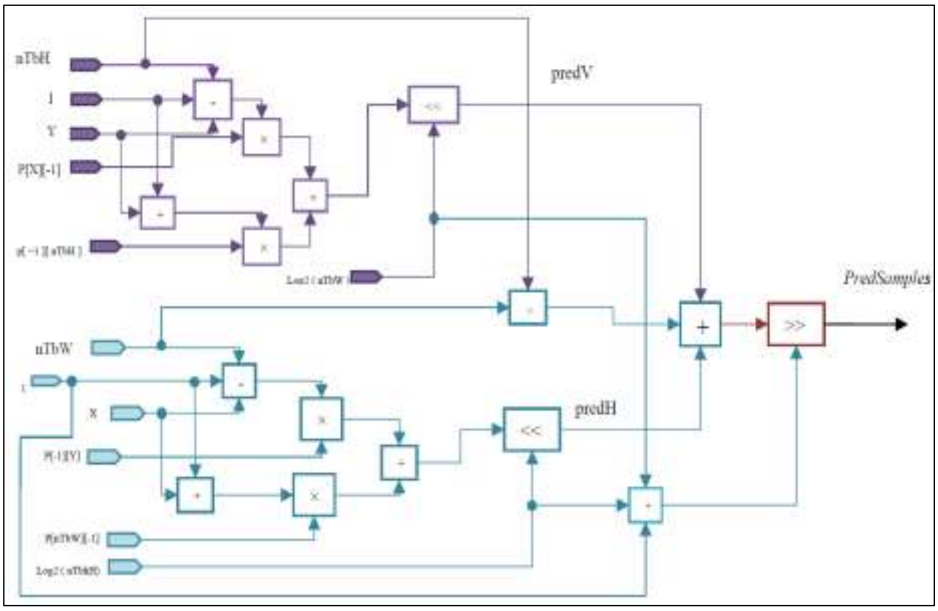

Figure 5: Proposed architecture of Planar VVC intra prediction.
Source: Authors, (2025).

III.5 PROPOSED DESIGN OF CONTROL PATH FSM prediction

The control step of our proposed algorithm of intra prediction modes is based on Finite State Machine (FSM) and is charged to manage the generation of predsamples for the four modes in VVC standard. This FSM Prediction is constructed with twelve 12 transition States as shown in Figure 10. Each transition state is reserved to control and manage the following operations:

- ✓ State 1: is charged to initialize the VVC intra prediction algorithm;
- ✓ State 2: is charged to initialize the prediction modes for chroma samples;
- ✓ State 4: is charged to initialize the prediction modes for luma samples;
- ✓ State 21 to state 24: are reserved to control the 4 prediction modes (DC, Planar, Angular and CCLM modes) respectively;
- ✓ State 31 to state 32: activate and deactivate the Horizontal and Vertical directions for angular mode;
- ✓ State 33 to state 35: activate and deactivate the 3 CCLM modes (CCLM LT, CCLM L and CCLM T);
- ✓ Eni: activation signals for each step;
- ✓ Donei: deactivation signals for each step (end of process).

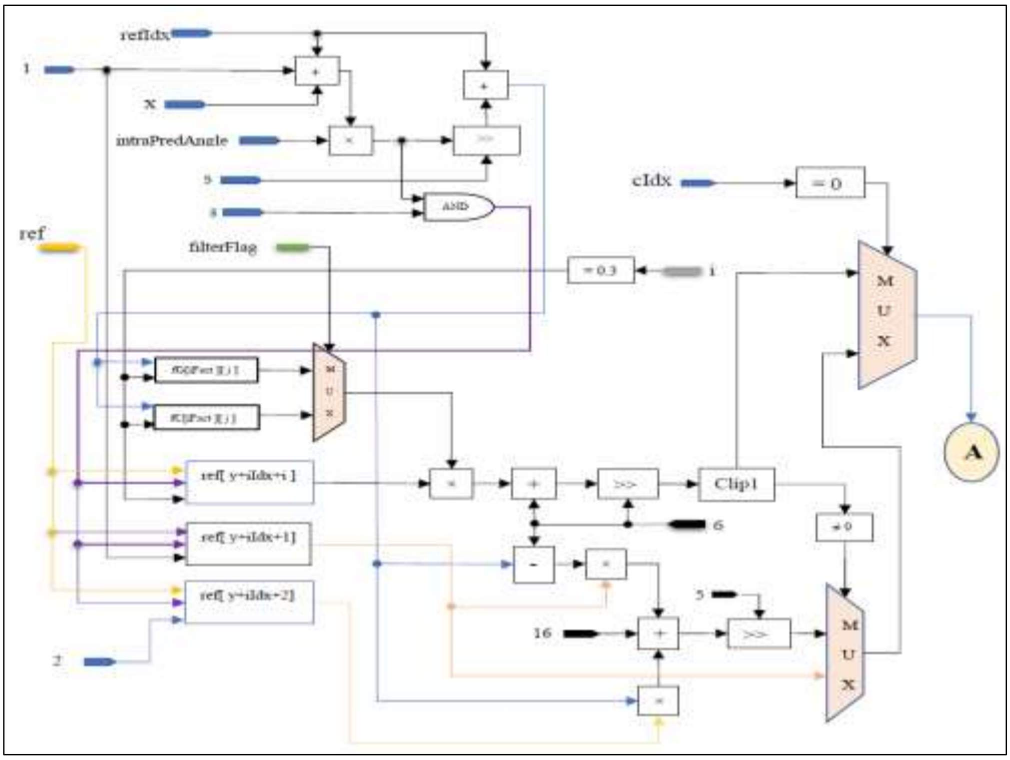

Figure 6: Block diagram showing Low-Level design of Angular part1 mode in VVC intra prediction.
Source: Authors, (2025).

IV. EXPERIMENTAL RESULTS

This work is described in VHDL language of ISE description environment, targeted an FPGA device Virtex 7 version and simulated on ModelSim. Moreover, the structural and behavioral architectures are adopted for both data flow and control flow.

IV.1 SYNTHESIZED RESULTS OF OUR WORK

Table.2 listed the synthesized results of VVC intra prediction modes designs separately. We can see clearly that the CCLM mode consumes more resources compared to the other modes namely: angular, planar and DC. Moreover, the CCLM and the angular use the same number of DSP Block and BRAM components. According to listed values in this table, we can see that angular and CCLM modes designs consume more resources compared to DC and Planar designs especially the Digital signal processing (DSP) blocks. Hence, it is signaled that DSP48E1 blocks are used in cases that contain operands multiplication, addition and subtraction of large sizes numbers (25 x 18 bits for multiplier, 25 bits for adder and subtractor).

Table 2:The synthesized results of DC, Planar, Angular and CCLM prediction modes designs.

	Slice	LUT	Slice FF	BRAM	DSP Block
DC mode	24	22	47	1	0
Planar mode	27	25	216	1	0
Angular mode	23	15	295	2	20
CCLM mode	33	18	370	2	10
Clause.6.4.4	45	21	98	0	2

Source: Authors, (2025).

IV.2 COMPARISON RESULTS OF OUR DESIGN OF VVC INTRA PREDICTION MODE

In Table 3, we compare our proposed results of FPGA implementation of VVC intra prediction algorithm with those existing in literature. The works W1, W2, and W3 proposed partial intra prediction implementation with generation of only single samples per cycle against full implementation proposed in W4, W5, W7, and our work with multi-samples per cycle. Moreover, W1, W2, W4, W5, and W6 process the video data in HEVC codec, but our work and W3 are compatible to VVC codec. This implementation and all proposed works can used 4 to 32 PUs sizes and support all angular direction (33 directions for HEVC and 65 directions for VVC). W4 and W6 give high throughput of 2800 Samples/s and 1200 Samples/s respectively for HEVC codec which are greater than that given by our proposed work; otherwise, the resources are really very important that can reach 31200 LUTs in W4 compared to our work with only 12000 LUTs and can generate a good prediction throughput about 1068 Samples/s and in VVC codec. The area efficiency of our architecture is equal to 0.089 Samples/s/LUTs which is the better one compared to all proposed VVC intra prediction implementation. The only work where that obtains the same value of area efficiency is W4; however, this work proposed full HEVC intra prediction with three modes of prediction: DC, planar, and angular compared to our implementation of full VVC intra prediction with four prediction modes: DC, Planar, angular, and the new one CCLM.

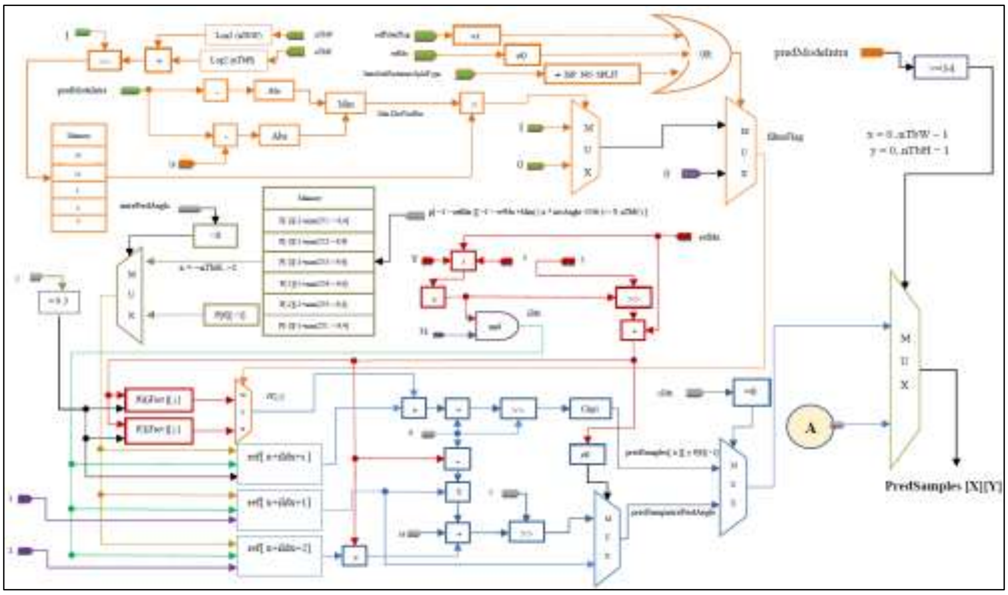

Figure 7: Block diagram showing Low-Level design of Angular part2 mode in VVC intra prediction.
Source: Authors, (2025).

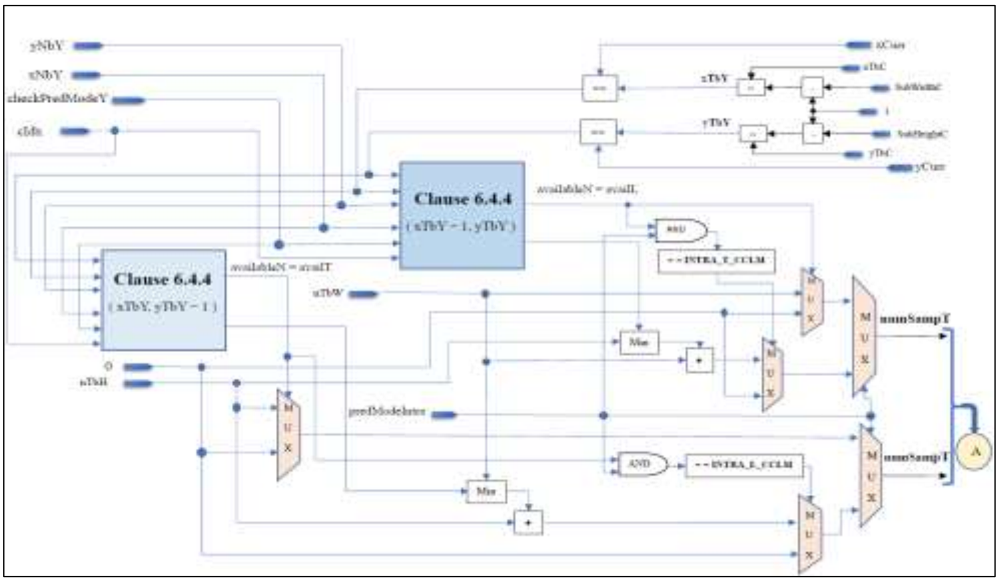

Figure 8: Block diagram showing Low-Level design of CCLM part1 mode in VVC intra prediction.
Source: Authors, (2025).

Table 3: Comparison of the proposed work with other similar works in literature.

Intra prediction works	W1 [12]	W2 [8]	W3 [11]	W4 [19]	W5 [20]	W6 [21]	Proposed Work
Year	**2017**	**2018**	**2019**	**2019**	**2020**	**2022**	**2025**
Intra prediction Version	**HEVC**	**HEVC**	**VVC**	**HEVC**	**HEVC**	**HEVC**	**VVC**
FPGA Technology	Virtex-6 (40nm)	Virtex-6 (40nm)	Virtex-7 (28nm)	Kintex-7 (28nm)	Kintex-7 (28nm)	Artix-7 (28nm)	Virtex-7 device
PU Size	4, 8, 16, 32	4, 8, 16, 32	4, 8, 16, 32	4, 8, 16, 32	4, 8, 16, 32	4, 8, 16, 32	4, 8, 16, 32
Directional mode	All	All	All	All	All	All	All
Samples/cycle	1	1	1	16	8	8	6
Frequency (MHz)	250	227	119	175	110	150	178
Throughput (Samples/s)	250	227	NA	2800	880	1200	1068
BRAMs	3 Kb	4 Kb	3.2 Kb	62 Kb	NA	NA	4 BRAMs
Blocks DSP	NA	10	60	NA	40	40	32
Resources (LUTs)	6013	4425	46382	31200	16000	16200	12000
Full intra prediction modes	Partial (Angular)	Partial (Angular)	Partial (Angular)	Full Intra modes	Full Intra modes	Full Intra modes	Full Intra modes
Area Efficiency (Samples/s/ LUTs)	0.041	0.051	NA	0.089	0.055	0.074	0.089

Source: Authors, (2025).

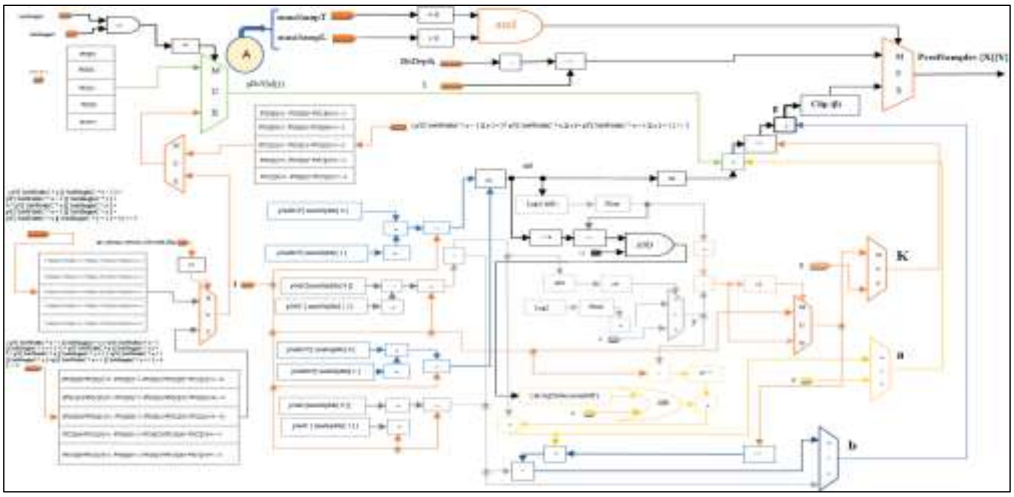

Figure 9: Block diagram showing Low-Level design of CCLM part2 mode in VVC intra prediction.
Source: Authors, (2025).

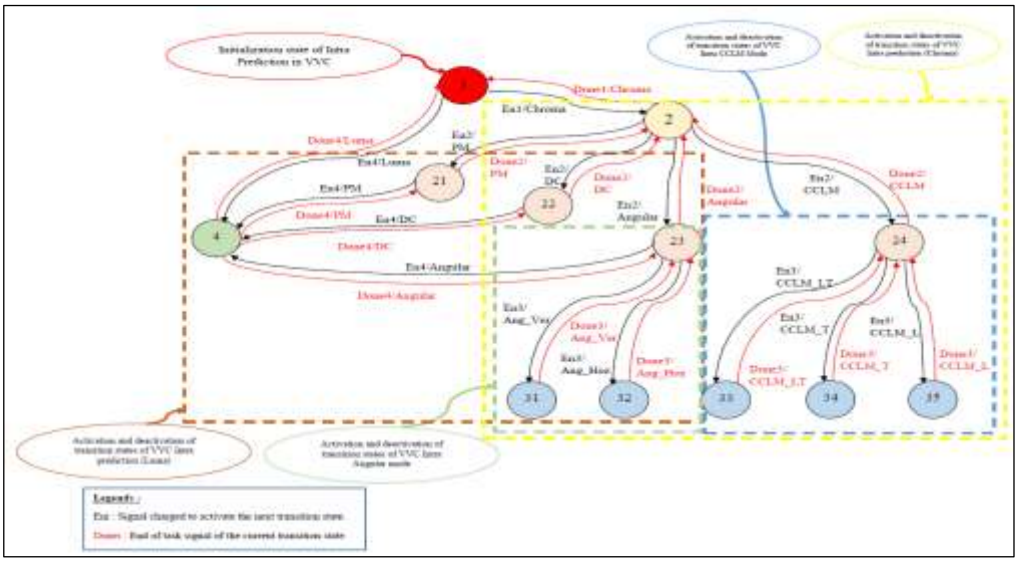

Figure 10. Block diagram showing Low-Level design of control path FSM Prediction Modes.
Source: Authors, (2025).

V. CONCLUSIONS

In this work, a new parallel architecture of VVC intra prediction algorithm is proposed implemented on FPGA device and can process multi-samples per cycle. Two different optimization techniques are adopted in this work namely: parallelism to improve the throughput and memory rearrangement to increase the number of block RAM. So, we have designed, implemented and simulated the four prediction modes separately: DC, Planar, Angular and the newest CCLM modes in order to verify the good functioning of each of them before passing to the Full intra prediction architecture. The synthesized results show that our full intra prediction architecture can process 6 predicted samples per cycle and operate at frequency of 178 MHz. Moreover, a good value of throughput is obtained, which is about 1068 samples/s with acceptable number of resources in terms of 12000 LUTs. The area efficiency is the better one compared to all works in literature of Full VVC intra prediction with value of 0.089 Samples/s/LUTs. Furthermore, this work is the only which presents an efficient FPGA implementation of VVC intra prediction algorithm with full prediction modes. As perspectives, we are going to realize an FPGA implementation of intra VVC encoding algorithm with low energy consumption.

VI. AUTHOR'S CONTRIBUTION

Conceptualization: Mukanda Kere Wanyama, Michael Nakitare Waswa and Linda Ouma.
Methodology: Mukanda Kere Wanyama, Michael Nakitare Waswa and Linda Ouma.
Investigation: Mukanda Kere Wanyama, Michael Nakitare Waswa and Linda Ouma.
Discussion of results: Mukanda Kere Wanyama, Michael Nakitare Waswa and Linda Ouma.
Writing – Original Draft: Mukanda Kere Wanyama, Michael Nakitare Waswa and Linda Ouma.
Writing – Review and Editing: Mukanda Kere Wanyama, Michael Nakitare Waswa and Linda Ouma.
Resources: Mukanda Kere Wanyama, Michael Nakitare Waswa and Linda Ouma.
Supervision: Mukanda Kere Wanyama, Michael Nakitare Waswa and Linda Ouma.
Approval of the final text: Mukanda Kere Wanyama, Michael Nakitare Waswa and Linda Ouma.

VII. REFERENCES

[1] Telecommunication standardization sector of ITU: Series H: Audiovisual and multimedia systems, Infrastructure of audiovisual services-Coding of moving video (Versatile video coding), H.266, V3, 09/2023.

[2] Uhrina, Miroslav Sevcik, Lukas Bienik, Juraj Smatanova, Lenka. (2024). Performance Comparison of VVC, AV1, HEVC and AVC for High Resolutions. doi:10.20944/preprints202402. 0869.v1.

[3] H. Chen, T. Zhang, M. -T. Sun, A. Saxena and M. Budagavi, "Improving Intra Prediction in High-Efficiency Video Coding," in IEEE Transactions on Image Processing, vol. 25, no. 8, pp. 3671-3682, Aug. 2016, doi:10.1109/TIP.2016.2573585.

[4] J. Pfaff et al., "Intra Prediction and Mode Coding in VVC," in IEEE Transactions on Circuits and Systems for Video Technology, vol. 31, no. 10, pp. 3834-3847, Oct. 2021, doi: 10.1109/TCSVT.2021.3072430.

[5] Telecommunication standardization sector of ITU: Series H: Audiovisual and multimedia systems, Infrastructure of audiovisual services-Coding of moving video (High efficiency video coding), H.265 12/2016.

[6] Xin Li, Simeng Sun, Zhizheng Zhang, Zhibo Chen; Multi-Scale Grouped Dense Network for VVC Intra Coding, Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR) Work-shops, 2020, pp. 158-159.

[7] J. Pfaff et al., "Intra Prediction and Mode Coding in VC," in IEEE Transactions on Circuits and Systems for Video Technology, vol. 31, no. 10, pp. 3834-3847, Oct. 2021, doi: 10.1109/TCSVT.2021.3072430.

[8] X. Zhao, V. Seregin, A. Said, K. Zhang, H. E. Egilmez and M. Karczewicz, "Low-Complexity Intra Prediction Refinements for Video Coding," 2018 Picture Coding Symposium (PCS), San Francisco, CA, USA, 2018, pp. 139-143, doi: 0.1109/PCS.2018.8456305.

[9] M. Sch¨afer et al., "Efficient Fixed-Point Implementation Of Matrix-Based Intra Prediction," 2020 IEEE International Conference on Image Processing (ICIP), Abu Dhabi, United Arab Emirates, 2020, pp. 3364-3368, doi: 10.1109/ICIP40778.2020.9190883.

[10] H. Azgin, A. C. Mert, E. Kalali and I. Hamzaoglu, "An efficient FPGA implementation of HEVC intra prediction," 2018 IEEE International Conference on Consumer Electronics (ICCE), Las Vegas, NV, USA, 2018, pp. 1-5, doi: 10.1109/ICCE.2018.8326332.

[11] H. Azgin, E. Kalali and I. Hamzaoglu, "An Efficient FPGA Implementation of Versatile Video Coding Intra Prediction," 2019 22nd Euromicro Conference on Digital System Design (DSD), Kallithea, Greece, 2019, pp. 194-199, doi: 10.1109/DSD.2019.00037.

[12] H. Azgin, E. Kalali and I. Hamzaoglu, "A computation and energy reduction technique for HEVC intra prediction," in IEEE Transactions on Consumer Electronics, vol. 63, no. 1, pp. 36-43, February 2017, doi: 10.1109/TCE.2017.014728.

[13] E. Kalali and I. Hamzaoglu, "FPGA implementation of HEVC intra prediction using high-level synthesis," 2016 IEEE 6th International Conference on Consumer Electronics - Berlin (ICCE-Berlin), Berlin, Germany, 2016, pp. 163-166, doi: 10.1109/ICCE-Berlin.2016.7684745.

[14] Kammoun, M., Ben Atitallah, A., Ben Atitallah, R., Masmoudi, N. (2017). Design exploration of efficient implementation on SoC heterogeneous platform: HEVC intra prediction application. International Journal of Circuit Theory and Applications, 45(12), 2243-2259. DOI:10.1002/cta.2308.

[15] M. Kammoun, A. Ben Atitallah and N. Masmoudi," An optimized hardware architecture for intra prediction for HEVC," International Image Processing, Applications and Systems Conference, Sfax, Tunisia, 2014, pp. 1-5, doi: 10.1109/IPAS.2014.7043303.

[16] Z. Pan et al.," Efficient Chroma Intra Prediction via Exemplar Colorization Network for Versatile Video Coding," in IEEE Transactions on Multimedia, doi: 10.1109/TMM.2025.3535312.

[17] A. Filippov, V. Rufitskiy, and J. Chen, "CE3-related: Alternative techniques for DC mode without division, Document JVET-K0122 of JVET, July 2018.

[18] Luo, Dan Xiong, Shuhua Ren, Chao Sheriff, Ray He, Xiaohai. (2022). Fusion-Based Versatile Video Coding Intra Prediction Algorithm with Template Matching and Linear Prediction. Sensors. 22. 5977.10.3390/s22165977.

[19] Ding, D., Wang, S., Liu, Z., Yuan, Q., Real-Time, H.: 265/HEVC Intra Encoding with a Confgurable Architecture on FPGA Platform. Chin. J. Electron. 28, 1008–1017 (2019).

[20] Poola, L., Aparna, P.: A Mixed Parallel and Pipelined Efcient Architecture for Intra Prediction Scheme in HEVC. IETE Tech. Rev., 1–13 (2020).

[21] Poola, L., Aparna, P. An efficient parallel-pipelined intra prediction architecture to support DCT/DST engine of HEVC encoder. J Real-Time Image Proc 19, 539–550 (2022). https://doi.org/10.1007/s11554- 022-01206-2.