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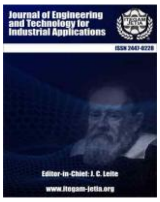

RESEARCH ARTICLE

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INPUT CURRENT RIPPLE REDUCTION OF MODIFIED INTERLEAVED QUADRATIC BOOST CONVERTER FOR PHOTOVOLTAIC APPLICATIONS

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ABSTRACT

In photovoltaic (PV) systems, achieving high voltage gain and keeping low input current ripple is essential for reliable operation and ensuring that the PV source consistently provides its maximum power. Low input current ripple helps the PV module operate close to its maximum power point (MPP). Conventional DC converters including quadratic boost converter frequently exhibit significant input current ripple for constrained voltage gain. To improve performance under varying load and irradiance conditions, a modified interleaved quadratic boost converter (MIQBC) is suggested. The proposed converter is able to reduce the input current ripple by employing a two-phase interleaved structure that operates with a 180° phase shift, incorporating design modification. Using an ESP32 control unit and a perturb and observe (P&O) algorithm to control the maximum power point during operation. The converter was simulated with LTspice, designed, and tested practically to assess the performance under real solar irradiation. The theoretical analysis indicated that the voltage gain reached approximately four times the input voltage, and input current ripple reduced to less than 2% while the efficiency was about 96% at full load. The experimental tests indicated that the converter demonstrated reliable performance and effective power tracking by eliminating the input current ripple. The topology provides high reduction in input current ripple and a real enhancement in voltage gain compared to conventional topologies. The results ensure efficient use of the PV panel's maximum power capability and proves that the converter is suitable for photovoltaic applications.

I. INTRODUCTION

Renewable energy technologies have been dramatically improved as sustainable substitutes for fossil fuels in recent years [1], [2] . Given the drawbacks of using fossil fuels to generate electricity, such as the possibility of ongoing climate change brought on by increased greenhouse gas emissions from burning them as fuel, it would not be wise to use them to supply power [3]. Photovoltaic power is regarded as one of the most attractive electrical power generating methods since sunlight, which is required to generate electricity, is available year-round and worldwide [4-7]. The output voltages of these energy sources, such as fuel cells and solar panels fluctuating [8], [9]. Therefore, a high-ratio DC-DC converter is required to regulate the produced voltage or tracking the maximum power [10], [11]. On the contradiction, conventional boost converters must operate at extremely high duty-cycle ratios to provide a high output voltage, which is practically difficult to achieve because of high combined losses and semiconductors limitations [12]. Likewise, as illustrated in Figure 1, High input current ripple from high ON periods prevents the PV from operating at maximum power point and causes it to oscillate around it, which increases system losses due to the additional heating in the PV and switching elements all these factors reduce the efficiency of the system [13], [14]. However, for continuous PV output energy, a large capacitor is required, or a continuous current converter can be used. Adding a C or LC filter can reduce reliability, increase weight and volume, cause electrical resonance problems, and cost money, especially when electrolytic capacitors are included [15-18].

To attain a high output voltage with a suitable duty ratio, a number of high step-up converters have been proposed. A new quadratic boost converter is shown in [19]. it's a three-stage converter based on a single-switch quadratic converter, voltage lift technique (VL) with voltage multiplier cell (VMC). Voltage lift cell has a simple construction, can improve its gain with an average duty cycle, and can also reduce the power switch's voltage stress to half the output voltage of the converter. This allows for using MOSFET with a lower voltage rating, which reduces conduction losses and lowers costs. A novel quadratic boost single-switch coupled inductor CI [20]. It has a continuous and low input current ripple; for achieving ultra-high output voltage, a VMC is connected to the converter. Furthermore, there is a passive clamp capacitor connected in parallel with the power switch to limit the voltage stress on it by recycling the magnetic energy in the CI, which causes a significant voltage spike in the switching component.

To reduce losses and improve efficiency, it's important to know that a passive clamp is used instead of an active one because of its simplicity and minimal effect on the control system. A new modification of the DC-DC quadratic boost converter can be found in [21]. It is a mixture between a Cuk and a conventional boost converter, so there are two stages with two power switches. The first stage is made by the Cuk converter to achieve continuous input current. The second stage consists of the conventional BC, which doubles the gain and produces an output voltage with positive polarity. So, with this technique, the voltage conversion ratio will be high (quadratic of a conventional converter) without needing to operate with a high duty ratio as in a conventional boost converter. A novel topology of interleaved quadratic boost converters with VM has been proposed [22] This converter consists of two stages.The first stage contains two QBCs connected in parallel, which is known as the interleaved QBC.

The interleaving led to an increase in the frequency of the converter and made it possible to filter with small capacitors. This property makes smooth input current compared with the conventional converter, so the input current ripple will reduce with interleaving, and this optimizes the input current magnitude for the maximum power point algorithm. The second stage is a Dickson voltage multiplier cell that cascades with the first stage. This VMC helps achieve a high voltage gain by increasing the voltage conversion ratio. A developed topology from the QBC is shown in [23]. It's a high step-up converter that depends on a 2-phase interleaved quadratic boost converter using multi-winding CIs instead of discrete inductors; this change in the inductor type facilitates achieving a light and compact magnetic element and helps in reducing the input current ripple. To achieve more gain, it's connected to a voltage lift capacitor and a VMC. A new topology of interleaved non-isolated high-gain converters has been proposed [24].

It provides a high voltage gain without having to work with a high duty cycle. This improvement in gain is due to using two three-winding coupled inductors with two circuits of VMC. High gain is attained through the adjustment of the turn's ratio of these inductors, which reaches 16% more than similar boost topologies. A Modified Interleaved Quadratic Boost Converter (MIQBC) is suggested as a solution to the mentioned constraints. The converter achieves a high step-up voltage gain appropriate for PV systems while eliminating the input current ripple by modifying an interleaved two-phase structure with 180° phase-shifted operation. The main objective of this work is to show that this converter is efficient through theoretical design, simulation with LTspice, and experimental verification. The proposed converter provides enhanced maximum power extraction and reduced ripple compared to traditional topologies. The research utilizes the perturb and observe (P&O) method within an ESP32-based MPPT control system to guarantee its optimum performance across different conditions.

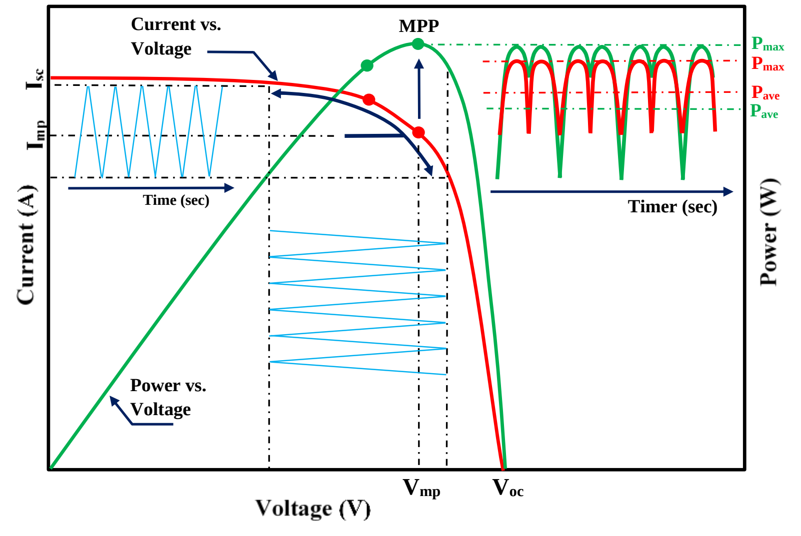


Figure 1: The impact of ripple in input current on the PV power curve.
Source: Authors, (2026).

II. CONVERTOR DESIGN AND CONFIGURATION

The proposed converter is based on the quadratic boost converter. It is a two-phase interleaved QBC with a modification in its design that reduces the input current ripple. Each phase consists of a single power switch, four diodes, two capacitors and two inductors. This interleaving helps to reduce the input current ripple. The modification is represented by replacing the inductors' positions and using the inductor of the high inductance in the input side, which causes additional reduction in the input current ripple instead of using a capacitor in the input. Also, to avoid the flow of (D_2, D_5) current to the capacitors (C_1, C_2) during the transient duration, an additional diode has been added (D_7, D_8). The configuration circuit of the proposed converter is shown in Figure 2.

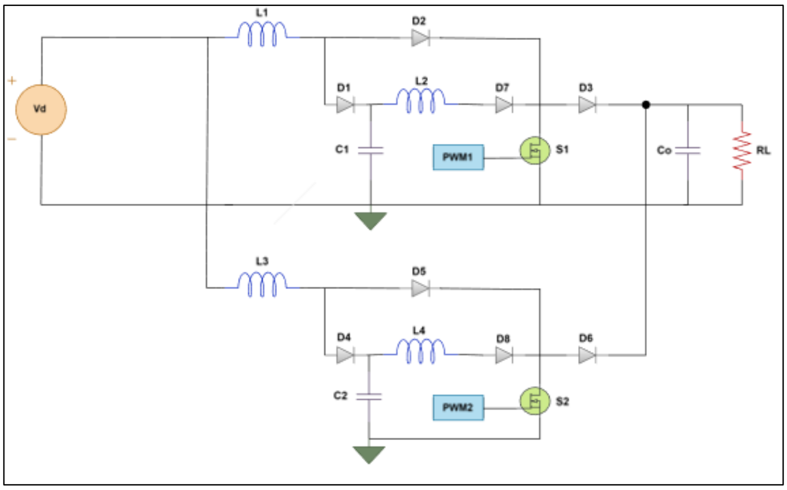


Figure 2: The proposed converter.
Source: Authors, (2026).

II.1 PRINCIPLE OF OPERATION

As mentioned, the MIQBC consists of two identical quadratic boost converters connected in series on the output side while connected in parallel on the input side, and these converters operate with a phase shift of 180° between the drive signals of their switch gates to verify that when one switch is ON, the other is in the opposite state for a portion of the cycle. Also, to maintain proper interleaving operation and prevent overlap between the conduction intervals, the operation duty ratio should be kept below 0.5 per channel. There are four modes of operation during the complete interval of switching, all explained under the assumption that the operation is in steady-state conditions, all circuit devices are ideal, the capacitor sizes are sufficient to maintain a constant voltage across their terminals, the inductors are energised before the switches turn on and designed for operation in continuous conduction mode (CCM). The voltage and current waveforms of this operation are shown in Figure 3.

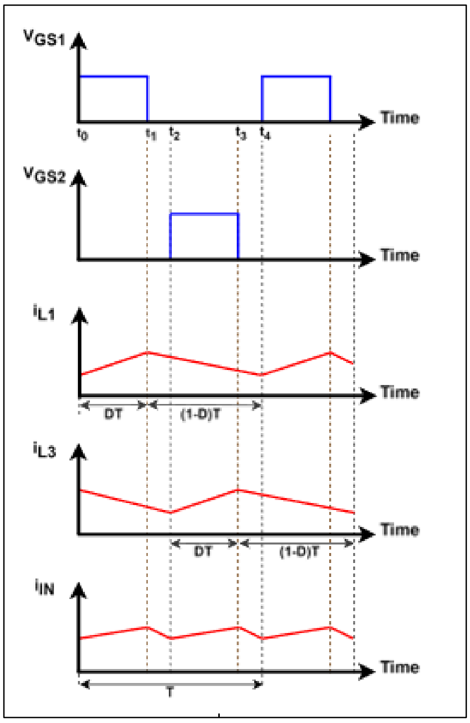


Figure 3: The steady state operation waveforms.
Source: Authors, (2026).

Mode I: (S_1 ON, S_2 OFF)

This mode is shown in Figure 4(a) when the converter operates during the interval from t_0 to t_1.
(a) The first-phase inductors L_1 and L_2 store energy from the input source and C_1 respectively.
(b) The second-phase inductors L_3 and L_4 transferred their stored energy to charge C_o and supply the load.

Mode II: (S_1 OFF, S_2 OFF)

This Mode shown in Figure 4(b) when the converter operates during the interval from t_1 to t_2.

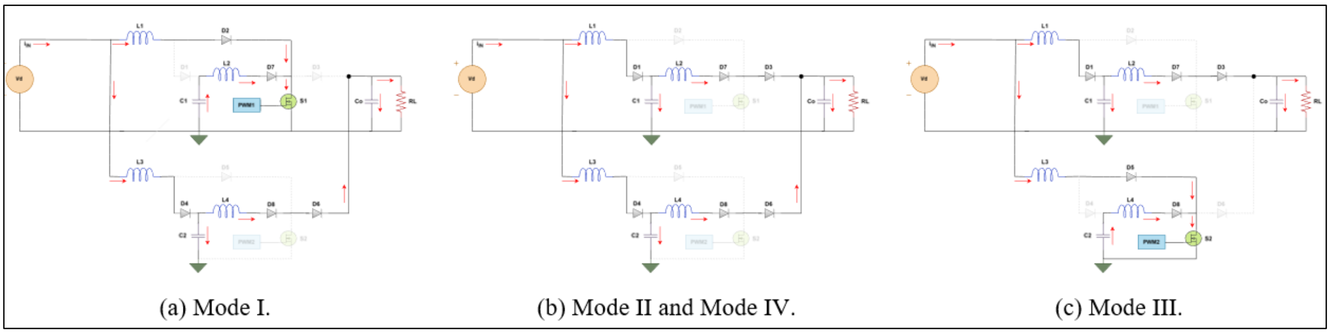
(a) The first-phase inductors L_1 and L_2 transferred their stored energy to charge C_o and supply the load.
(b) The second-phase inductors L_3 and L_4 remain in their status in Mode I.

Mode III: (S_1 OFF, S_2 ON)

This Mode shown in Figure 4(c) when the converter operates during the interval from t_2 to t_3.
(a) The first-phase inductors L_1 and L_2 remain in their status in Mode II.
(b) The second-phase inductors L_3 and L_4 store energy from the input source and C_2 respectively.

Mode IV: (S_1 OFF, S_2 OFF)

This Mode is typical of Mode II and shown in Figure 4(b) when the converter operates during the interval from t_3 to t_4.
(a) The first-phase inductors L_1 and L_2 remain in their status in Mode III.
(b)The second-phase inductors L_3 and L_4 transferred their stored energy to charge C_o and supply the load.

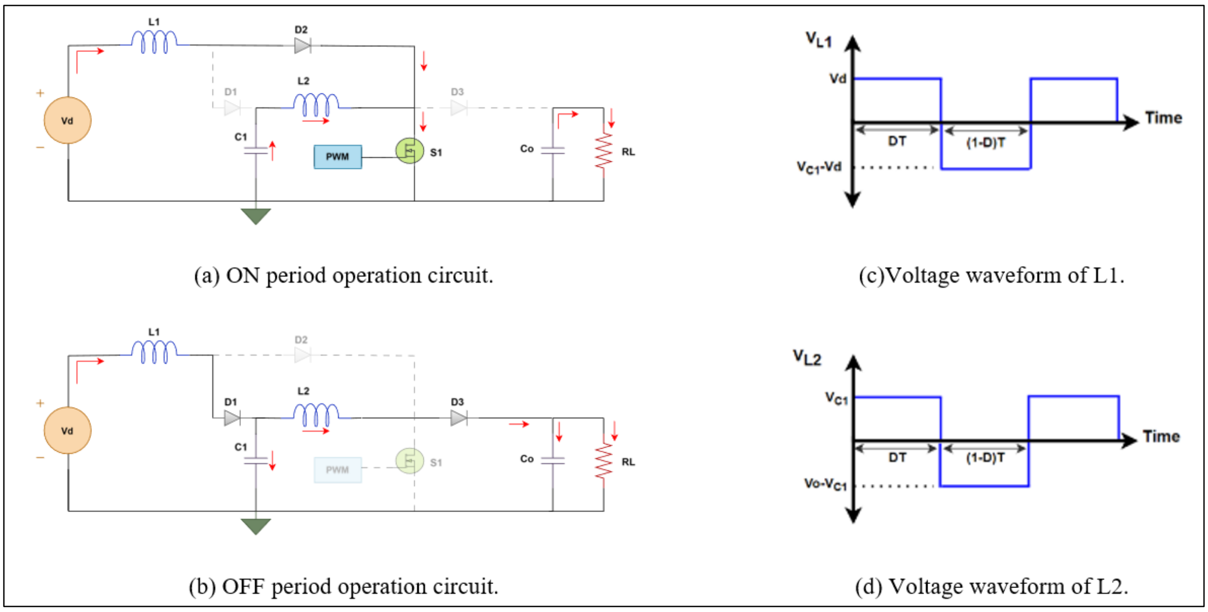


(a) Mode I. (b) Mode II and Mode IV. (c) Mode III.

Figure 4: The steady state operation Modes.
Source: Authors, (2026).

II.1.1 Voltage Conversion Ratio

The steady state analysis of this convertor based on the conventional quadratic boost convertor shown in Figure 5 So, the voltage conversion ratio (M) calculated from the inductor's voltages V_{L1} and V_{L2} under the assumption of constant input voltage, ideal switches and purely resistive load. As a result of volt-second balance, the integral of V_{L1} and V_{L2} over one time period is equal to zero [25], [26]. Figure 5 shows the circuit operation and the inductor's voltage waveforms.



(a) ON period operation circuit. (c)Voltage waveform of L1.

(b) OFF period operation circuit. (d) Voltage waveform of L2.

Figure 5: Convertor operation.
Source: Authors, (2026).

$$\int_0^{Ts} V_{L1} = 0 \tag{1}$$

$$(V_d)DT = (1-D)T(V_{C1} - V_d)$$

$$\therefore \ \frac{V_{C1}}{V_d} = \frac{1}{(1-D)}$$

$$\int_0^{Ts} V_{L2} = 0 \tag{2}$$

$$(V_{C1})DT = (1-D)T(V_O - V_{C1}) \qquad \therefore \frac{V_{C1}}{V_O} = (1-D)$$

$$\text{So, the voltage conversion ratio} \qquad M = \frac{V_O}{V_d} = \frac{1}{(1-D)^2}$$

Also, as shown in Figure 6, the integral of each capacitor current during one switching time period is zero at steady state [26].

$$\int_0^{Ts} i_{C1} = 0 \tag{3}$$

$$(I_{L2})DT = (I_{L1} - I_{L2})(1-D)T \qquad I_{L2} = (1-D)I_{L1} \tag{4}$$

$$\int_0^{Ts} i_{C2} = 0 \tag{5}$$

$$(I_O)DT = (I_{L2} - I_O)(1-D)T$$

$$(I_O)DT = (I_{L2} - I_O)(1-D)T$$

$$I_O = (1-D)I_{L2} \tag{6}$$

$$I_O = (1-D)^2 I_{L1} \tag{7}$$

To find the inductors current ripple [27]

$$V_{L1} = L_1 \frac{dIL_1}{dt} \qquad \therefore \Delta I_{L1} = \frac{DTV_d}{L_1}$$

$$V_{L2} = L_2 \frac{dIL_2}{dt} \qquad \therefore \Delta I_{L2} = \frac{DTV_{C1}}{L_2}$$

Now to find the critical values of the inductors to operate in CCM [27]:

$$I_{L1} \geq \frac{\Delta I_{L1}}{2} \qquad \therefore L_1 \geq \frac{(1-D)^4 DR_L}{2f_s}$$

$$I_{L2} \geq \frac{\Delta I_{L2}}{2} \qquad \therefore L_2 \geq \frac{(1-D)^2 DR_L}{2f_s}$$

To find the capacitors voltage ripple [27]

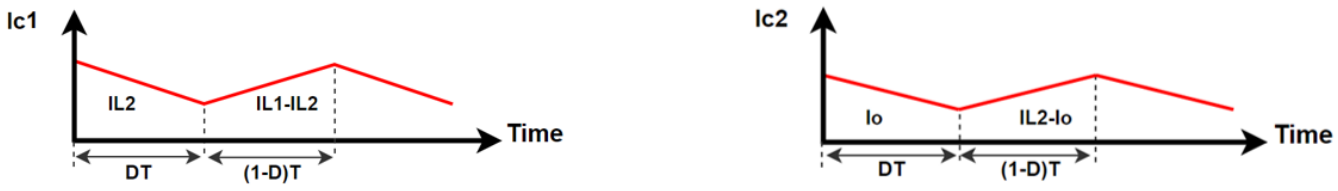
$$\Delta V_{C1} = \frac{\Delta Q_{C1}}{C_1} \qquad \therefore \Delta V_{C1} = \frac{DTV_o}{(1-D)C_1 R_L}$$

$$\Delta V_{Co} = \frac{\Delta Q_{Co}}{C_o} \qquad \therefore \Delta V_{Co} = \frac{DTV_o}{C_o R_L}$$

Now to find the inductors current ripple ratio and the capacitors voltage ripple ratio:

$$\rho_{L1} = \frac{\Delta I_{L1}}{I_{L1}} = \frac{(1-D)^4 DTR_L}{L_1} \qquad \rho_{L2} = \frac{\Delta I_{L2}}{I_{L2}} = \frac{(1-D)^2 DTR_L}{L_2}$$

$$\rho_{C1} = \frac{\Delta V_{C1}}{V_{C1}} = \frac{DT}{(1-D)^2 C_1 R_L} \qquad \rho_{Co} = \frac{\Delta V_{Co}}{V_{Co}} = \frac{DT}{C_o R_L}$$



(a) Current waveform of C_1.

(b) Current waveform of C_2.

Figure 6: Capacitors' current waveforms.
Source: Authors, (2026).

II.1.2 Voltage Stress Across Semiconductor Devices

Since the proposed two-phase MIQBC is developed from a classical QBC and the switches are located at the output end of each QBC structure, the voltage impressed across them is obtained as:

$$V_{S1} = V_{S2} = \frac{V_{in}}{(1-D)^2} = V_O \tag{8}$$

The reverse voltage applied across the diodes indicates their voltage rating. When S_1 and S_2 are ON, diodes D_1 and D_4 are, respectively, reverse-biased; their voltage rating determined from the potential difference across their anode and cathode terminals. The cathode terminal of D_1 is clamped at the voltage level of C_1, while the anode terminal is grounded through D_2 and S_1. Interestingly, the voltage developed across C_1 is the same as that of a CBC. Similar factors can be used to determine the voltage stress on D_4. Therefore, the voltage stress on D_1 and D_4 is determined as:

$$V_{D1} = V_{D4} = \frac{V_{in}}{(1-D)} = V_O(1-D) \tag{9}$$

The voltage stress on diodes D_2 and D_5 is obtained when the switches S_1 and S_2 are in the OFF state, respectively. The cathode of D_2 is clamped by the voltage developed across the positive plate of C_o through D_3, while the anode of D_2 experiences the potential developed across C_1. Diode D_5 is located at a position which is similar to D_2. Hence, its voltage stress is the same as D_2. Therefore, the net voltage stress is derived as:

$$V_{D2} = V_{D5} = \frac{V_{in}}{(1-D)^2} - \frac{V_{in}}{(1-D)} = \frac{V_{in}D}{(1-D)^2} = V_O D \tag{10}$$

The voltage stress on diode D_3 is obtained when switch S_1 is ON and S_2 is in the OFF state. The cathode of D_3 is clamped by the voltage developed across the positive plate of C_o, while the anode terminal of D_3 is grounded through S_1. Therefore, the net voltage stress on D_3 is equal to V_o. Furthermore, the voltage stress on diode D_6 is obtained when switch S_1 is OFF and S_2 is in the ON state. The cathode of D_6 is clamped by the voltage developed across the positive plate of C_o, while the anode terminal of D_6 is grounded through S_2. Therefore, the net voltage stress on D_6 is equal to V_o.

$$V_{D3} = V_{D6} = \frac{V_{in}}{(1-D)^2} = V_O \tag{11}$$

There is no voltage stress on D7 and D8 because no reverse voltage is impressed across them.

II.1.3 Current Stress on Semiconductor Devices

The current stress on the switches S_1 and S_2 is determined when they are in ON state. When S_1 is ON, the inductors L_1 and L_2 charge through D_2, D_7 and S_1. Hence, the current flowing through the switch is the sum of the inductor currents I_{L1} and I_{L2}. Thus, the current stress on S_1 is given by:

$$I_{S1} = I_{L1} + I_{L2} \tag{12}$$

Similar factors can be used to determine the current stress on the switch S_2 and is expressed as:

$$I_{S2} = I_{L3} + I_{L4} \tag{13}$$

Diodes (D_1, D_2, D_4, and D_5) are closer to the input side. so, their current-carrying capacity needs to be closer to the magnitude of input current. Fortunately, as an interleaved structure is employed, the total current is shared. The current stress on diodes D_1 and D_2 is the same as the inductor current I_{L1}, whereas diodes D_4 and D_5 are rated to carry the current flowing through inductor L_3. The diode current stresses are expressed as:

$$I_{D1} = I_{D2} = I_{L1} = \frac{I_{in}}{2} \tag{14}$$

$$I_{D4} = I_{D5} = I_{L3} = \frac{I_{in}}{2} \tag{15}$$

D_3 and D_6 are the regular output rectifier diodes. Hence, the current stress on them is the same as the output current. Also, for D_7 and D_8 located closer to the output side. Therefore, their current-carrying capacity needs to be closer to the output current magnitude and is given by:

$$I_{D3} = I_{D6} = I_{D7} = I_{D8} = I_o \tag{16}$$

II.1.4 Efficiency Analysis

Power loss occurring in DC resistance of inductor is:

$$P_{core} = \sum_{i=1}^{\varnothing} k\, f_s^{\alpha}\, B_{ipk}^{\beta}\, V_{icore} \tag{17}$$

P_{core} core losses, Ø number of inductors, f_s switching frequency, B_{pk} Peak flux density, V_{core} Core volume, (k, α, β) Steinmetz coefficients (from core datasheet).

$$P_{copper} = \sum_{i=1}^{\varnothing} I_{Li(rms)}^{2} \times DCR_i \tag{18}$$

$I_{L(rms)}$ is the inductor RMS current, *DCR* is the DC resistance of the inductor. So, the total inductors losses are:

$$P_L = P_{core} + P_{copper} \tag{19}$$

Switching and conduction loss in MOSFET is:

$$P_{Qsw} = \sum_{i=1}^{2} \frac{1}{2} V_{iDS} I_{iD} (t_r + t_f) f_s \tag{20}$$

V_{DS} Drain-to-source voltage during switching, I_D Drain current of the MOSFET, t_r Current rise time during turn-on transition, t_f Current fall time during turn-off transition.

$$P_{Qcond} = \sum_{i=1}^{2} I_{i(rms)}^{2} \times R_{iDS(on)} \tag{21}$$

I_{rms} is the RMS current flowing through the MOSFET, $R_{DS(on)}$ On-state drain-to-source resistance of the MOSFET.

Power loss of in diode and capacitor is:

$$P_D = \sum_{i=1}^{N} I_{iD(avg)} V_{if} + \sum_{i=1}^{N} I_{iD(rms)}^{2} R_{iD} \tag{22}$$

N is the number of diodes, $I_{D(avg)}$ Average forward current of the diode, V_f Forward voltage drop of the diode, $I_{D(rms)}$ RMS current of the diode, R_D Dynamic (on-state) resistance of the diode.

$$P_C = \sum_{i=1}^{Z} I_{ic(rms)}^{2} ESR_i \tag{23}$$

Z is the number of capacitors, $I_{c(rms)}$ RMS ripple current of the capacitor, ESR_i Equivalent series resistance of the capacitor.

The total power loss is:

$$P_{Loss} = P_L + P_{Qsw} + P_{Qcond} + P_D + P_C \tag{24}$$

Efficiency of the converter is:

$$\%\eta = \frac{P_O}{P_O + P_{Loss}} \times 100 \tag{25}$$

II.2 COMPONENT DESIGN

To design the values for the proposed converter component, there are several factors to consider, like the operation frequency, the range of the duty cycle, the PV specification, and the load that is connected to the converter. It is necessary to know that at a low duty cycle (less than 0.2), the converter's low voltage gain has resulted in inefficient operation. While the duty cycle should not exceed 0.5 to avoid the overlap between the conduction intervals, the efficiency is also affected due to the increase in the diode's reverse recovery and the switches conduction losses. The values of the inductors and capacitors, as well as the appropriate load connecting to this converter for testing, should now be determined. Assume that the converter is operating at D = 0.5 and the switching frequency is $f_s = 90\ KHz$, and that it is connected to a PV with the specifications listed in Table 1.

Table 1: PV data sheet.

PV Specifications	Values
Rated maximum power P_{max}	250 W
Voltage at P_{max} (V_{mp})	30.1 V
Current at P_{max} (I_{mp})	8.30 A
Open-circuit voltage (V_{oc})	37.2 V
Short-circuit current (I_{sc})	8.87 A
Nominal operating Cell Temp (NOCT)	25° C

Source: Authors,(2026).

To determine this PV cell's equivalent circuit: $I_{ph} \cong I_{sc} \cong 8.87\ A$

$$R_s = \frac{V_{oc}-V_{mp}}{I_{mp}} = 0.855\ \Omega \qquad R_{sh} = \frac{V_{oc}}{I_{sc}-I_{mp}} = 65.26\ \Omega$$

In the theoretical derivations, a duty cycle of D=0.5 was selected. This value corresponds to the theoretical upper limit for the chosen converter design and provides accurate estimations of current/voltage stresses.

$$M = \frac{V_o}{V_{in}} = \frac{1}{(1-D)^2} \qquad V_o = \frac{30.1}{(1-0.5)^2} \cong\ 120\ Volt$$

For efficiency of 96%:

$$P_{max} = V_{mp}\, I_{mp} =\ 250\ W \qquad P_o = 0.96\ x\ 250\ =\ 240\ W$$

$$P_o = \frac{V_o^2}{R_L} \qquad \therefore R_L = \frac{(120)^2}{240} = 60\ \Omega$$

The above data can now be used to compute the inductors' critical values.

$$L_1 \geq \frac{(1-D)^4 D R_L}{2 f_s} \geq 10.416\ \ \mu H \qquad L_2 \geq \frac{(1-D)^2 D R_L}{2 f_s} \geq 41.66\ \mu H \qquad \therefore \frac{L_1}{L_2} \cong \frac{1}{4}$$

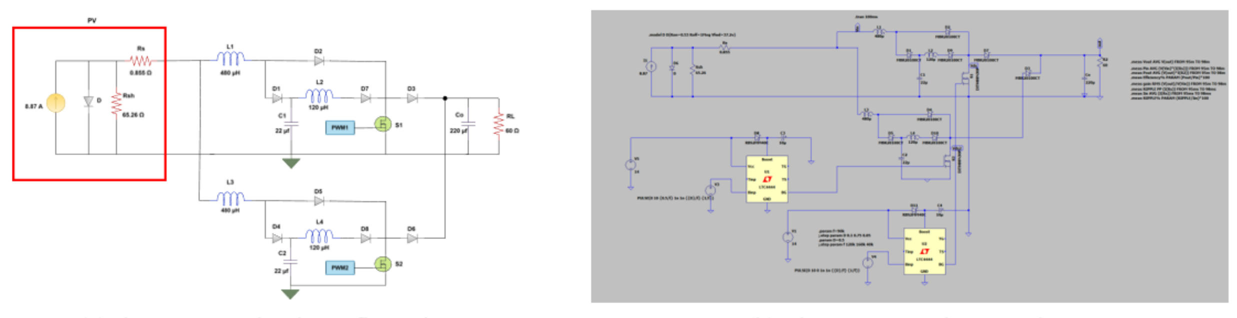
For a given voltage and switching frequency, the current ripple (ΔI) in an inductor is inversely proportional to the inductance (L) $\Delta I_L = \frac{DTV}{L}$. Therefore, it is easy to see that a higher value of L results in a lower input current ripple, but at the expense of efficiency. Increasing the inductance (L) of an inductor will typically reduce the ripple of current in a circuit. After testing various inductor values using LTspice, including (L_1=30 µH, L_2=120 µH),(L_1=60 µH, L_2=240 µH), (L_1=120 µH, L_2=480 µH), and (L_1=150 µH, L_2=600 µH), the decision was made to choose L1=120 µH, L2=480 µH, which is adequate to minimize input current ripple while maintaining a high efficiency value and Ensures that the converter operates in CCM even with changes in frequency.he value of the capacitors must be chosen to have low voltage ripple: $\rho_{C1}<10\%$, $\rho_{Co}<0.1\%$

$$\frac{DT}{(1-D)^2 C_1 R_L} < 10\% \qquad C_1 > 3.704\ \mu f$$

$$\frac{DT}{C_o R_L} < 0.1\% \qquad C_o > 92.59\ \mu f$$

The capacitors' value can be adjusted set as: $C_1 = 22\ \mu f\ , C_2 = 220\ \mu f$

The theoretical derivations prove that the QBC (quadratic boost convertor) is a multiplication of two stages of BC (boost convertor) ($M = \frac{1}{(1-D)}$), as can be seen from the voltage conversion ratio of the QBC ($M = \frac{1}{(1-D)^2}$). This led to a modification that will help to further reduce the input current ripple by using the stage of the higher inductance L as an input stage, as illustrated in Figure 7, which represents the MIQBC (modified interleaved quadratic boost converter).



(a)The MIQBC circuit configuration. (b) The MIQBC using LTspice.

Figure 7: The proposed topology circuit.
Source: Authors, (2026).

III. PRACTICAL DESIGN AND EXPERIMENTAL SETUP

In this section, we applied the proposed converter in practice to verify its operation and assess its effectiveness in reducing the input current ripple for maximum power point tracking. As illustrated in Figure 8, to track the maximum power of the converter, perturb and observe (P&O) method has been adopted. Input voltage and current are measured continuously by voltage and current sensing circuits, which then send these signals to the ESP32 microcontroller to apply the maximum power point algorithm shown in the flow chart of Figure 9, which determines the value of the duty cycle. So, ESP32 generates two PWM signals with a 180° phase shift at a certain duty cycle to supply the drive circuit, which controls the operation of the MOSFET to drive the converter.

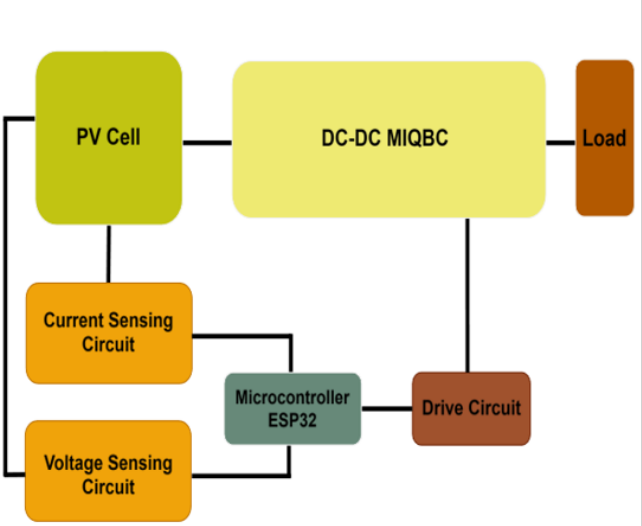


Figure 8: Close loop MIQBC.
Source: Authors, (2026).

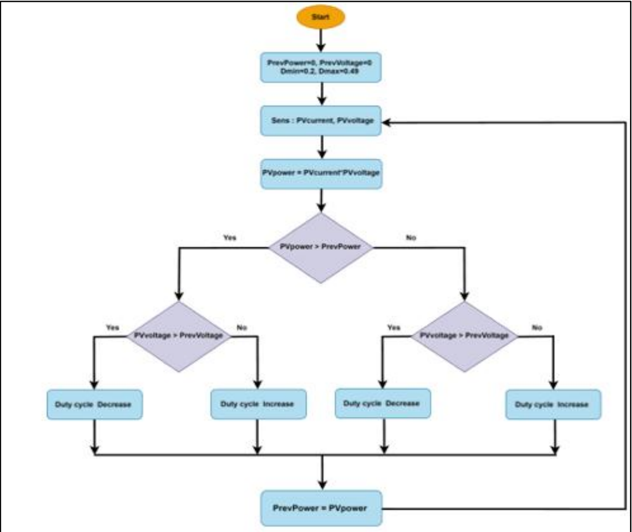


Figure 9: MPPT algorithm flowchart.
Source: Authors, (2026).

The proposed converter is practically designed using components and devices that were available in the laboratory. It is important to mention that some alternative components were used to obtain approximate results. The hardware setup consists of the following main components:

•**Power MOSFETs:** Two IRF260N transistors, due to their low on-resistance and high current capability.

•**Diodes:** MBR20100CT Schottky diodes, for low forward voltage drop and fast switching.

•**Inductors:** Iron Powder Core type T157-26, suitable for high-frequency DC-DC converter applications.

•**Capacitors:** High-frequency capacitors for output filtering.

•**Gate Driver Circuit:** The IR2110 is used to drive the MOSFET by providing proper gate signals for the interleaved switches.

•**Control Unit**: An ESP32 microcontroller was used to implement the MPPT control algorithm and to generate interleaved PWM signals with a phase shift of 180°.

- **Sensing Circuits:** Voltage and current sensing circuits were designed to measure PV input current and voltage for real-time feedback to the control system.

- **Load:** Four resistive loads of 15 Ω / 100 W each were connected in many ways to achieve different loads and test various operating conditions.

- **Power Supply:** The input of the converter was supplied from a photovoltaic (PV) source with specifications almost similar to the one used in simulation. While a 12 Volt DC supply was used to power the driver circuit.

- **Measurement Instruments:** To verify the converter's functionality, switching waveforms, input/output voltages, and currents were recorded using an oscilloscope.

IV. RESULTS AND DISCUSSIONS

This section shows the simulation results using LTspice and compares them with the experimental results of the practical design.

IV.1 SIMULATIONS RESULTS

Using the LTspice program, simulate the IQBC with various values for L_1, L_2, L_3, and L_4 to select suitable inductance values by comparing input current ripple percentage and efficiency, as illustrated in Figure 10. Then modify it to obtain the MIQBC and compare it with many conventional topologies (boost converter, quadratic boost converter) to see the effect of these modifications as shown in Figure 11.

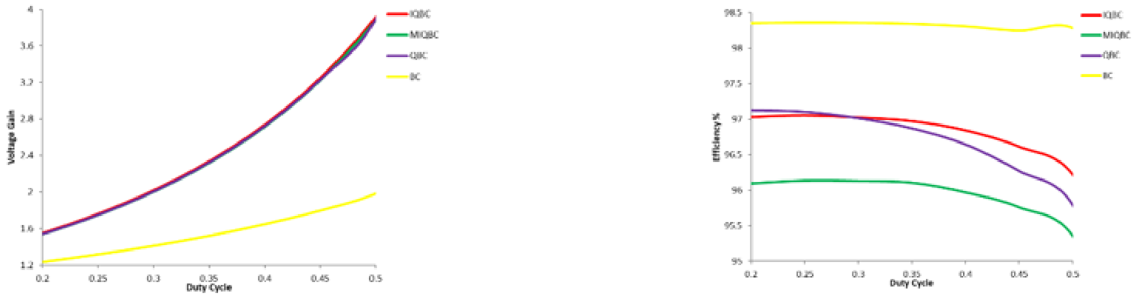
(a) IQBC ripple% with duty cycle.

(b) IQBC efficiency with duty cycle.

Figure 10: IQBC with various inductances.
Source: Authors,(2026).

(a) Comparison in ripple%.

(b) Comparison in P_{IN}.

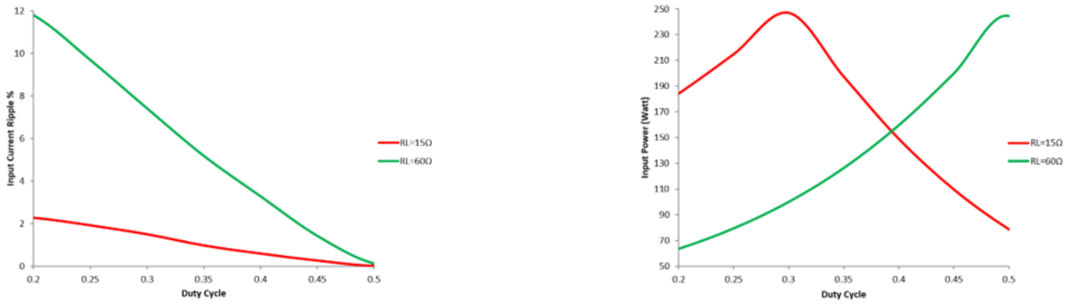


(c) Comparison in voltage gain.

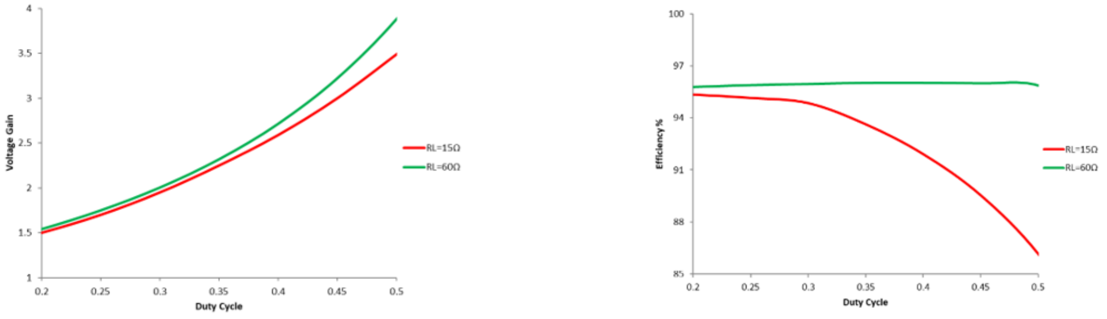
(d) Comparison in efficiency.

Figure 11: Converters comparison.
Source: Authors, (2026).

Once the values of ($L_1 = 120\ \mu H$ and $L_2 = 480\ \mu H$) have been accepted to be sufficient, use these values to simulate the MIQBC and compare it with other converters, as illustrated in Figure 11. When compared to other converters, the MIQBC offers a significant reduction in input current ripple, assisting in obtaining the maximum power possible from the PV. Although this adjustment had a minor impact on efficiency, it was still high, and the difference from other converters was insignificant. To evaluate how well the suggested converter performs when the load ($R_L = 15\ \Omega$) changes compared to it with the previous load, as illustrated in Figure 12. In order to achieve maximum input power, the MIQBC operates at a different duty cycle (D ≅ 0.32), which is practically adjustable according to the MPPT algorithm.



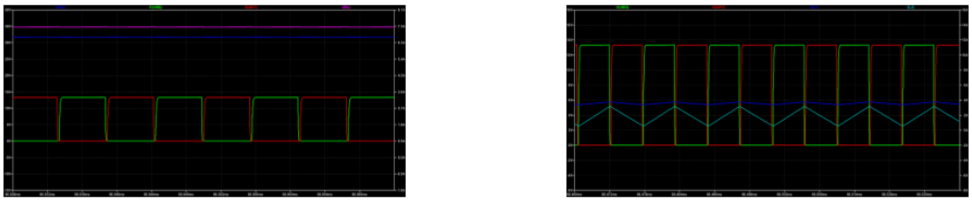
(a) Load comparison in ripple%. (b) Load comparison in P_{in}.



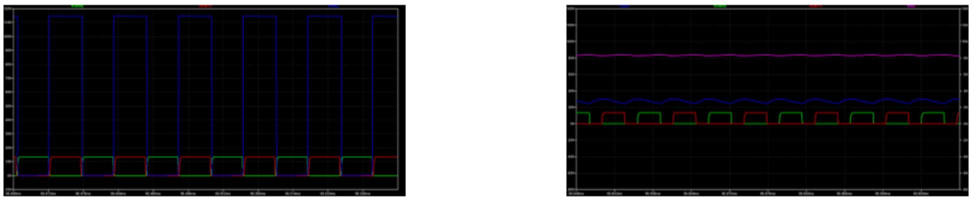
(c) Load comparison in voltage gain. (d) Load comparison in efficiency.

Figure 12: Load comparison.
Source: Authors, (2026).

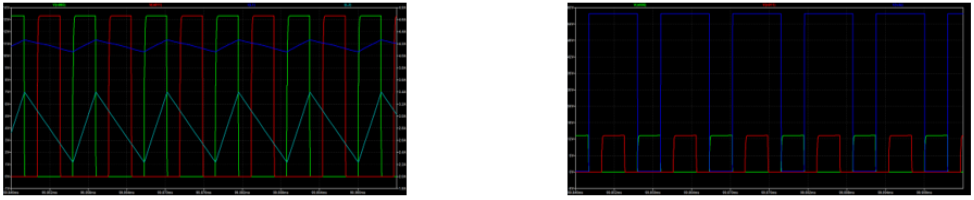
Finally, Figure 13 shows that the current and voltage waveforms of the MIQBC using LTspice at duty cycles of 0.5 and 0.32 were cleared. All these simulation results will be compared with the practical work results to verify the converter's operation and to prove its effect in the input current ripple reduction.



(a) I_{in} & V_{in} with PWM signals at R_L=60 Ω. (b) I_{L1} & I_{L3} with PWM signals at R_L=60 Ω.



(c) V_{ds} with PWM signals at R_L=60 Ω. (d) I_{in} & V_{in} with PWM signals at R_L=15 Ω.

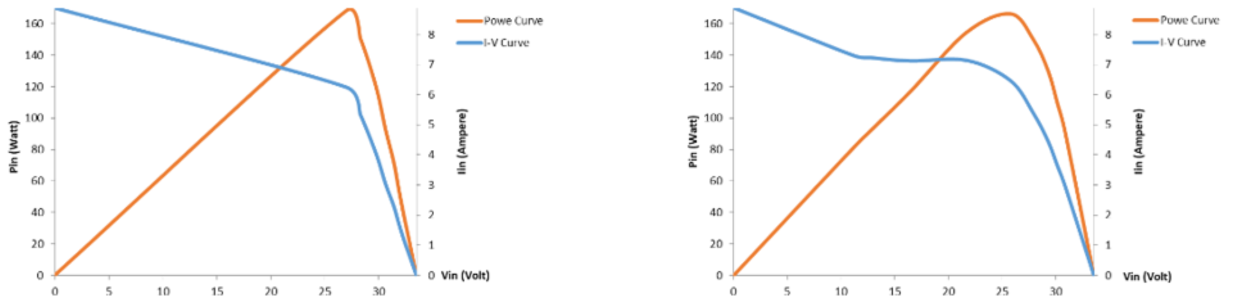


(e) I_{L1} & I_{L3} with PWM signals at R_L=15 Ω. (f) V_{ds} with PWM signals at R_L=15 Ω.

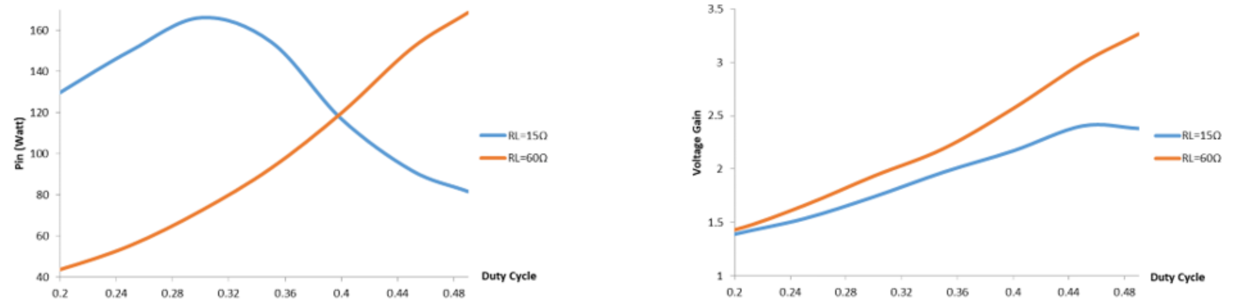
Figure 13: Simulation waveforms.
Source:Authors, (2026).

IV.2 EXPERIMENTAL RESULTS AND DISCUSSION

To distinguish the performance of the proposed converter under the test conditions. Initially it was a test without applying the MPPT algorithm by applying different values of duty cycle under the operation range (from 0.2 to 0.49) to draw the I-V curve for the PV cell under different load conditions by taking (R_L=60 Ω, R_L=15 Ω) as taken in the simulation. Figure 14 shows the curves that clarified the performance of the converter.



(a) I-V curve at R_L=60 Ω. (b) I-V curve at R_L=15 Ω.



(c) Load comparison in input power. (d) Load comparison in voltage gain.

Figure 14: MIQBC operation test.
Source: Authors, (2026).

As shown in curves (a) and (b) from Figure 14 , the maximum power of the PV cell occurs at the knee point of the I-V curve under different load conditions, and this power can be achieved by adjusting the duty cycle for loads of 15 Ω and 60 Ω. Figure 14(c) indicates that at R_L = 15 Ω, the maximum power is achieved at D ≅ 0.32, while at 60 Ω, the maximum input power occurs at D ≅ 0.48; additionally, Figure 14(d) illustrates that voltage gain increases with an increase in D. These practical results are acceptable results compared with the simulation results. It is necessary to mention that this test was not conducted under standard conditions because the test was conducted at 9:00 a.m. with an ambient temperature of 46℃, the high temperature lowers the voltage output of the solar cells. Furthermore, the normal sun irradiation at 9 a.m. is less than the 1000 W/m² standard test condition.

The PV module delivered less power than its rated value due to a combination of these factors: high temperature, surface impurifications, and decreased sunshine intensity. This can be proved by checking the input current ripple of the converter by oscilloscope. After that, the MPPT algorithm shown in the flowchart cleared in Figure 9 was applied to make sure that the converter can adjust the duty cycle to operate at the maximum power point. The waveforms of Figure 15 show the performance of the operations. As seen from (a) and (f), there is a very high reduction in the input current ripple, which proves that this converter helps to achieve the maximum power available from the PV cell. At R_L=60 Ω, the MPPT algorithm adjusted the duty cycle at D=46.43%, which is approximately equal to the value of the previous test (without applying the algorithm), and the same with R_L=15 Ω (D=32.14%). this prove that the algorithm operates correctly.

Also as illustrated in (b) and (g), the current ripple of the main inductor (L_1 or L_3) has a significant value (for only one of the QBC). However, using the interleaving technique by using phase-shifted switching signals to operate several converter phases, the interleaving approach efficiently reduces the input current ripple. A smoother overall input current and improved converter performance are the results of this phase displacement, which partially cancels out the ripple components of each phase current. Waveforms of (c) and (h) shows the ripple of the second inductor (L_2 or L_4) in each stage, it has a high current ripple comparing with the main inductor (L_1 or L_3). So, this is the reason that leaded to did the modification of the proposed convertor. Normal switching behavior can be seen in the measured waveforms of the MOSFET V_{ds} and the output diode voltage in (d), (i), (e) and (j). Because of the circuit's parasitic capacitance and inductance, there are small voltage spikes and ringing during the transitions. These transients are acceptable and indicate proper switching operation of the converter.

(a) I_{in}&V_{in} at R_L=60 Ω. (b) I_{L1} at R_L=60 Ω.

(c) I_{L3} at R_L=60 Ω. (d) V_{Dout} at R_L=60 Ω.

(e) V_{ds} at R_L=60 Ω. (f) I_{in}&V_{in} at R_L=15 Ω.

(g) I_{L1} at R_L=15 Ω. (h) I_{L3} at R_L=15 Ω.

(i) V_{Dout} at R_L=15 Ω. (j) V_{ds} at R_L=15 Ω.

Figure 15: Practical waveformes.
Source: Authors, (2026).

V. COMPARATIVE ANALYSIS

To illustrate the benefits of the suggested converter, this section includes some comparisons with relevant recent topologies that have been documented in research. Table 2 compares the voltage conversion ratio, component count, input current ripple, voltage stress on switch, and efficiency of the suggested MIQBC with comparable converters, among other typical performance parameters.

Table 2: Comparison of existing converters with the proposed converter.

Topology	Number of Components				Voltage Gain	Input Current Ripple%	Voltage Stress on Switches	Voltage Stress on output diode	Efficiency
	Passive		Active						
	L+CL	C	D	S					
Proposed convertor	4+0	3	8	2	$\frac{1}{(1-D)^2}$	0.266%	V_o	V_o	95.8%
BC	1+0	1	1	1	$\frac{1}{1-D}$	18.4%	V_o	$V_{in}-V_o$	98.25
QBC	2+0	2	3	1	$\frac{1}{(1-D)^2}$	22%	V_o	V_o	95.4%
IQBC	4+0	3	6	2	$\frac{1}{(1-D)^2}$	3.5%	V_o	V_o	96.22%
[28]	0+2	4	4	2	$\frac{2+n}{(1-D)^2}$	15%	$\frac{V_o}{2+n}$	$\frac{1+n}{2+n}V_o$	96.3%
[29]	4+0	5	4	2	$\frac{2D}{(1-D)^2}$	10–25%	$\sqrt{\frac{LEVo^2}{R_L D^2 T_s}}$	V_o	96.2%
[30]	0+2	4	6	2	$\frac{2}{(1-D)^2}$	12.9%	$\frac{V_o}{2}$	V_o-V_{Clift}	92.49%
[31]	0+2	4	6	2	$\frac{2}{1-D}+\frac{N}{1-D}+\frac{2nk}{1-D}$	11.11%	$\frac{V_o}{2+N+2nk}$	$\frac{(2+N)V_o}{2+N+2nk}$	92%

Source: Authors, (2026).

VI. CONCLUSION

The theoretical and experimental results prove the effectiveness of the proposed Modified Interleaved Quadratic Boost Converter (MIQBC) for photovoltaic applications. Under full load conditions, the output voltage gain obtained approached four times the input voltage, which is an acceptable value compared with the theoretical estimation. Furthermore, the input current ripple was theoretically reduced to less than 2% and practically eliminated, which gives an indication that the interleaving technique was successful in distributing the input current between the inductors and lowering the pulsing behavior. The proposed topology provided better performance in terms of current quality and voltage gain when compared to conventional boost convertor, quadratic boost converter and IQBC.

Due to the reduction in input current ripple, the photovoltaic panel operates more efficiently by operating closer to its maximum power point. As shown by experimental testing, this reduction enhances the total power extraction from the PV source. Although the theoretical efficiency was estimated between 94% and 96% under different load conditions, however, using non-ideal components such as soldering boards, general-purpose wires, and the limited quality of the inductors and switches, the practical efficiency was slightly lower. even with these constraints, the converter maintained stable operation. These results considered that the MIQBC topology offers an efficient and reliable photovoltaic energy conversion solution. The combination of very low input current ripple, high voltage gain, and improved power extraction from the PV panel makes it very suitable for renewable energy systems.

VII. AUTHOR'S CONTRIBUTION

Conceptualization: Abdulkarim Laith Abdulkarim and Ali Hussein Al-Omari.
Methodology: Abdulkarim Laith Abdulkarim and Ali Hussein Al-Omari.
Investigation: Abdulkarim Laith Abdulkarim and Ali Hussein Al-Omari.
Discussion of results: Abdulkarim Laith Abdulkarim and Ali Hussein Al-Omari.
Writing – Original Draft: Abdulkarim Laith Abdulkarim.
Writing – Review and Editing: Abdulkarim Laith Abdulkarim and Ali Hussein Al-Omari.
Resources: Abdulkarim Laith Abdulkarim.
Supervision: Ali Hussein Al-Omari.
Approval of the final text: Abdulkarim Laith Abdulkarim and Ali Hussein Al-Omari.

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