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PERFORMANCE VALUATION OF ELECTRICAL CHARACTERISTICS FOR MOSFET DEVICE USING TCAD SOFTWARE

Zahra R. Mahmood[1], Amir M. Nory*[2] and Omar I. Alsaif[3]

[1, 2]Dept. of Medical Instrumentations Technologies, Polytechnic College Mosul, Northern Technical University, Mosul, Iraq.
[3]Dept. of Electronic and Communication Technologies, Polytechnic College Mosul, Northern Technical University, Mosul, Iraq.

[1]https://orcid.org/0009-0008-7895-5719, [2]https://orcid.org/0000-0001-7066-8274, [3]https://orcid.org/0000-0003-2832-7868

E-email: mti.lec141.zahra@ntu.edu.iq, *Amirnory@ntu.edu.iq, omar.alsaif@ntu.edu.iq

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ABSTRACT

MOSFET transistor is one of the most important and efficient components in modern electronic circuits due to its high efficiency and low power consumption. The performance of N-MOS and P-MOS transistor has been studied and analyzed by evaluating key electrical characteristics such as threshold voltage, drain current, (gate and drain) voltages, LDD (Lightly Doped Drain functions), PLDD (P-type Lightly Doped Drain) and DIBL (Drain-Induced Barrier Lowering). Simulation using Silvaco TCAD Program tools was employed to extract the device structure and current-voltage characteristics for both transistors. For N-MOS, it was observed that drain current (Id) grew linearly with expanding gate voltage (Vg) for different values of drain voltages (Vd), while for P-MOS the values were opposite. The Threshold Voltage for N-MOS transistor (Vt= 0.5V) while for P-MOS (Vt= -0.5V), The maximum current obtained is Id= 0.515 mA at Vd= 3.35 V for N-MOS and the highest current obtained is Id= -0.335 mA at Vd= -3.35 V for P-MOS, so N-MOS was faster than P-MOS, while P-MOS is considered complementary to N-MOS. The two transistors were combined for more low power dissipation and high performance.

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I. INTRODUCTION

Metal-Oxide Semi-conductor field-effect transistor (MOSFET) is an essential part of electronic circuits. Their importance has increased significantly with the proliferation of integrated and portable devices in the consumer electronics sector. Virtually every device on the market today contains these devices [1], [2]. MOSFET device considered the main element of any digital electronic circuit and one of the functional elements of any digital system, such as a microprocessor circuit, mobile devices and flash EEPROM technology [3], [4]. Therefore, accurately studying for behavior of MOS transistors is extremely important in the design of any digital systems and circuits [5].

For several years, mostly N-MOS logics were faster than: (P-MOS and C-MOS) logic, as electrons mobility is greater than that for holes, and it was more simples to implements, dissimilar than C-MOS circuit as both transistors must be performed. Nevertheless in N-MOS logic, static power dissipation happen that means dc current is important to pass across the logic gate regardless steady state output. CMOS logic was used to solve this issue Because of their greater operating speed and reduced static power dissipation, CMOS technology has supplanted N-MOS technology. P-type and N-type MOSFETS coupled in symmetrical and complementary pairs are currently a common application of CMOS technology.

Because of the combination of P-MOS and N-MOS, static power dissipation in CMOS logic is low because P-MOS creates a low resistance channel between its source and drain when a low gate voltage is employed, but N-MOS has a high resistance path even for a low gate voltage. CMOS logic also provides high noise immunity but has problems of tunneling leakage current (when MOSFET is scaled) and short channel effects occur [2],[6]. Over time, the planar MOSFET structure has gradually developed into the Fin FET, GAA MOSFET (nano-MOSFET), and double-gate MOSFET (DG-MOSFET).

The advanced structure offers greater controllability. In other words, the advanced structure uses less power when the transistor is off. As a result, a contemporary computer built with advanced structure uses less power, conserving battery life. In summary, great performance (high on-state current), low power consumption (low off-state current), and fast switching speed (low delay) are necessary for the future of transistors [7],[8].

This research presents a comprehensive study of the performance of N-MOS and P-MOS transistors, taking into account variations that occur during manufacturing processes, using Silvaco software and TCAD technology. Study impact of LDD – Lightly Doped Drain functions to mitigate short channel effects in MOSFETs. To reduce high electrical fields at the gate edge, which cause Hot Carrier Injection (HCI) damage to the silicon gate or gate oxide Increased electrical leakage and PLDD – P-type Lightly Doped Drain same function as LDD, but these are light P-grafted regions located before the primary Source/Drain implant (P++). DIBL (Drain-Induced Barrier Lowering) effect for different value of Vd for both transistors.

II. LITERATURE REVIEW

According to [5] simulated the fabrication process of a 65nm N-MOS transistor using Silvaco TACAD. The simulation results showed that short-channel effects, such as penetration, subthreshold current, substrate current, and gate current, increase with smaller device size. According to [9] added a specific graphene material to the Silvaco software and fabricated it using existing material parameters that closely resemble those of graphene. They concluded that a graphene channel field transistor (FET) could be an ideal replacement for conventional silicon MOSFET with a small channel length and could be used in high speed, low power application. In [3] design and simulation of a100 nm n-type MOSFET transistor using SILVACO ATLAS software.

Through this study, design and simulation at the nanoscale is extremely useful in the electronics industry to ascertain whether all requirements are acceptable for the sustainable design of integrated circuits before moving on to their successful implementation on a large scale. According to [10] simulated the structure of a 100 nm n-type MOSFET transistor at the device level through mathematical verification using Silvaco-TCAD software. The operating mechanisms of various MOS devices were analyzed and verified. According to [11] used machine learning to model MOSFET devices. They found that machine learning can be used to accurately estimate the transient characteristic curve of a MOSFET transistor using a Keras-type neural network based on geometric data.

III. MATHEMATIC ANALYSIS

MOSFET structure is manufactured by depositing or growing a dielectric layer, often made of silicon dioxide on top of a semiconductor substrate. The gate and semiconductor function as the electrodes in this configuration, which is comparable to a planar capacitor with a dielectric between them. When a voltage is applied to the gate the, electric field influences the charge distribution within the semiconductor [12], [13]. A robust conduction channel forms beneath the gate of a MOSFET transistor when the gate voltage rises above the threshold voltage. The characteristics of the MOSFET material mostly determine the threshold voltage. The resulting channel, which stretches between the source and the drain at low drain voltages, contain holes in a P-MOS transistor and electrons in an N-MOS transistor. In an N-MOS transistor, the source and drain are doped with n+ electrodes and a p-type substrate, while in a P-MOS transistor, the source and drain are p+ electrodes with an n-type substrate, which is often connected to the source [14], [15].

The gate electrode is then created by depositing a layer of metal or polycrystalline silicon over the dielectric. When a channel forms and there is a potential difference between the source and drain, current can flow between them. Depending on the gate, source, and drain voltage values, a MOSFET transistor's behavior can be classified into three operating regions: the cutoff region, the linear region, and the saturation area. When studying an N-MOS transistor with source and substrate grounding, the transistor is in the cutoff region when the gate-source voltage is less than the threshold voltage, where the current between the source and the drain is ideally zero, with the possibility of a sub-threshold current appearing as a result of the transfer of some high-energy carriers [16], [17]. The subthreshold current can be given as:

$$I_d \approx I_{D0} \exp\left((V_{GS} - V_T)/n\left(\frac{kT}{q}\right)\right) \tag{1}$$

Where:

I_d is the drain current.

I_{D0} is the drain current when VGS=VT.

k is the Boltzmann constant.

T is the Kelvin temperature

q is the electronic charge.

on the channel potential under the condition that n > 1. n represents the tilt factor of the transistor governed by the control of gate voltage.

N-MOS transistor in the linear region acts as a resistor when VGS>VT and VDS<VGS −VT. In this operational region the drain current ID is as follows:

$$I_D = \left(\frac{\mu_n C_{ox} W}{L}\right)\left((V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right) \tag{2}$$

Where:

μ_n is the electron mobility in the channel.

c_{ox} the capacitance of oxide per unit area.

W is the gate's width.

L is the gate's length.

The oxide capacitance per unit area C_{ox} can be expressed as follows:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{3}$$

Where:

ε_{ox} is the dielectric constant of the gate dielectric.

t_{ox} is the thickness of the gate dielectric.

The channel is pinched off from the drain side and the N-MOS is considered to be operating in the saturation region when VGS> VT and VDS ≥ (VGS −VT). The saturation region's drain current can be expressed as follows:

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2 \tag{4}$$

The N-MOS function as a perfect current source in the saturation region and is independent of the drain voltage, as demonstrated by the equation above. However, a phenomenon known as channel length modulation causes the drain voltage to alter the channel's effective length. The drain current is dependent on the drain voltage when channel length modulation is included, and it may be expressed as:

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \tag{5}$$

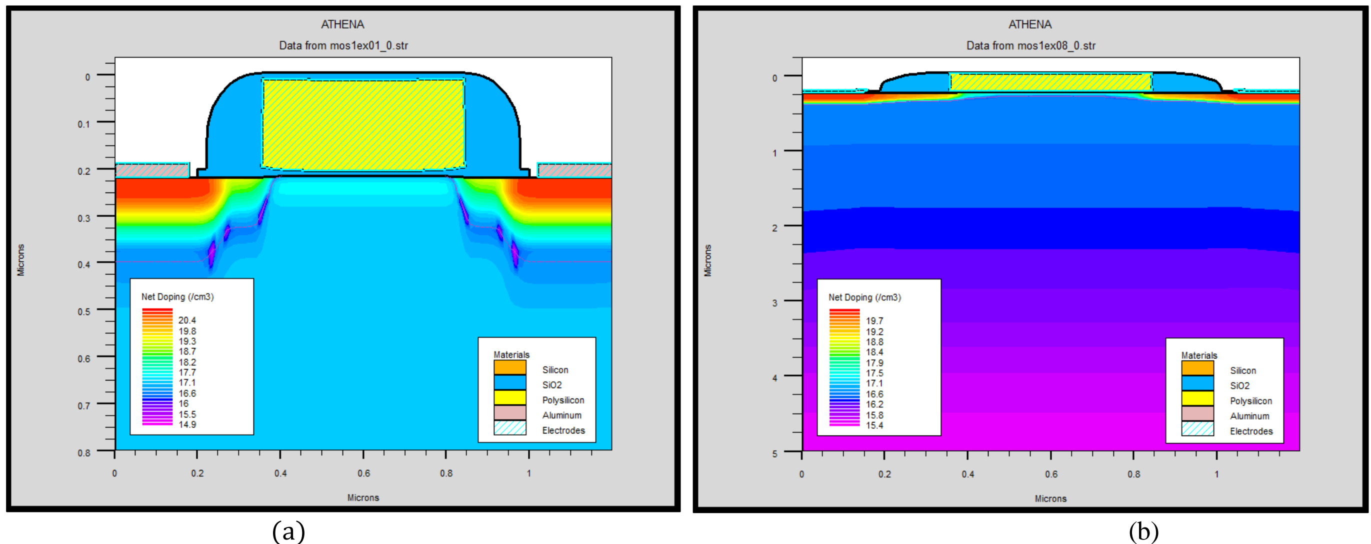
Where λ is the modulation parameter for channel length.

Is typically λ is proportional to the inverse of the channel length. The behavior of a P-MOS transistor are similar to the N-MOS where the source and substrate terminals are connected to the supply voltage except that the polarity of all the voltages and current reverse in the P-MOS, also the drain current in P-MOS primarily depends on the mobility of holes in the channel rather than the mobility of electrons [17-21].

IV. PRACTICAL SIMULATION AND RESULTS

Figure (1-a) shows the device structure for N-MOS transistor, which consists of; silicon layer at a bottom, P-well: Boron implanted under the channel and a thin layer of silicon dioxide (SiO2) was deposited as a boundary of the polysilicon gate. The source/drain (N++) zones and LDD zone between the channel and drain/source have Aluminum-metal contacts.

As shown in Figure(1-b) device-structure of P-MOS transistor, which consists of; silicon substrate, N-well: phosphorescently implanted to form the base of P-MOS channel, thin oxide layer between the gate and channel, and a Poly-silicon gate for the current control. PLDD/P++ source/ drain regions have a high impedance. Also, there is a spacer oxide layer used to isolate the gate from the field distribution and limit the LDD. Aluminum contacts used for electrical connection of the source/drain/gate.

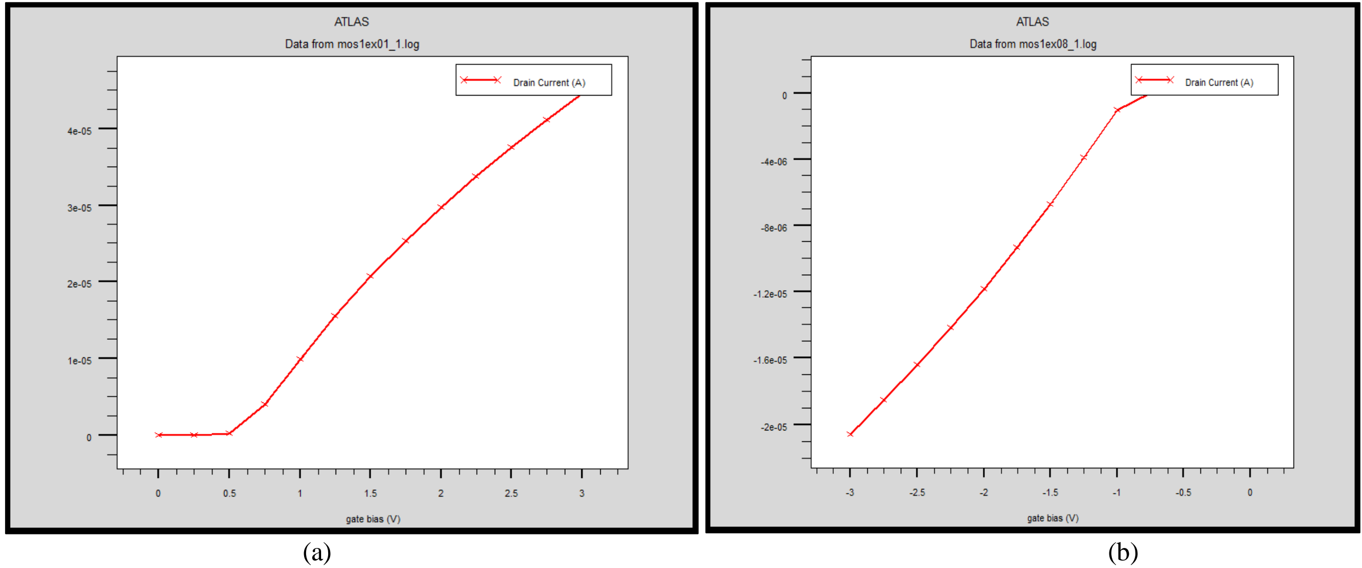


(a) (b)

Figure 1: device structure for MOSFET (a): N-MOS (b): P-MOS.

Source: Authors, (2026).

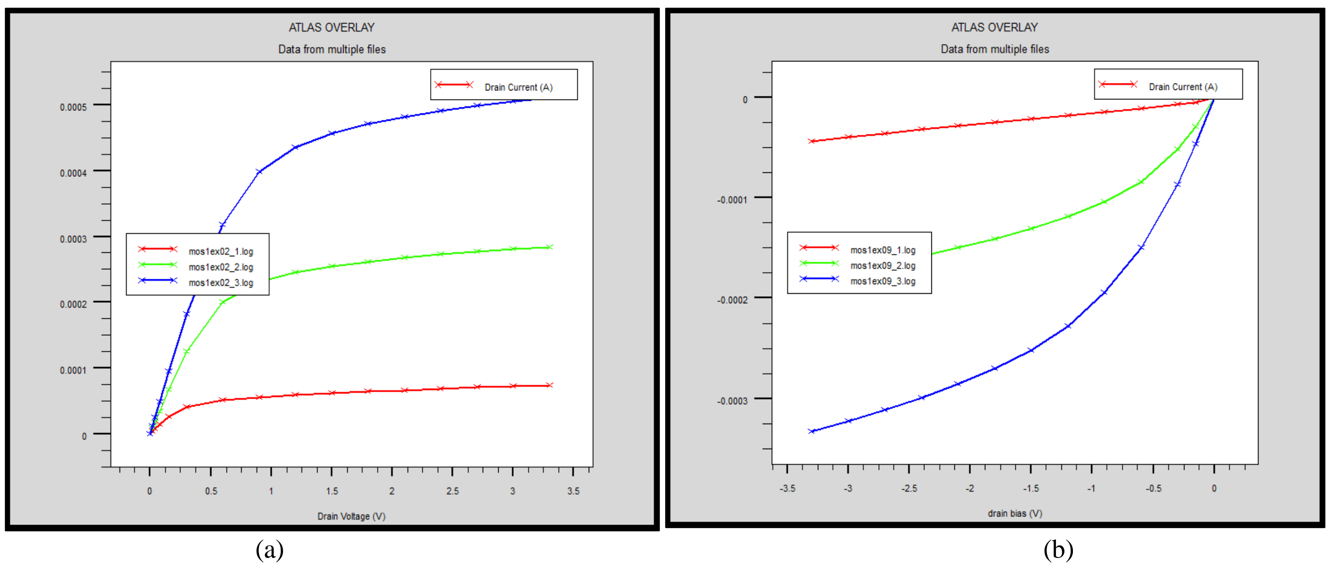
Figure (2-a) shows Id – Vg characteristics for N-MOS transistor, from the curve its observed that the current before Vt= 0.5V is very low almost zero, while this current increases linearly after the same Vt. Figure (2-b) shows the relation between Id and Vg for P-MOS transistor. From the curve, it is observed that the current starts from zero at Vg= 0V, and increases linearly at Vt= -0.5V, then reaches a very low value (-2*10-5 A) at Vg= -3V.



(a) (b)

Figure 2: Drain current vs. gate voltage (a): N-MOS (b): P-MOS.
Source: Authors, (2026).

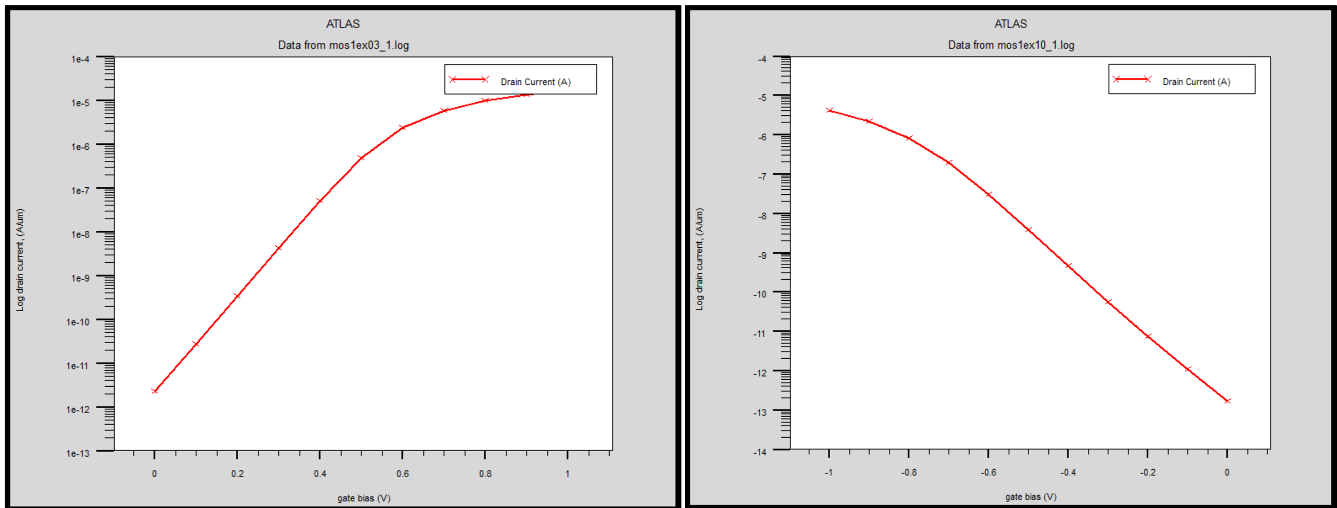
As shown in Figure (3-a) the Id vs. Vd properties for three values of Vg (1.1, 2.2, 3.3) V. It is observed that drain current (Id) grew linearly with expanding gate voltage (Vg) until it reaches saturation region at multi-values of Vd. The maximum current obtained is 0.515 mA at Vd= 3.35 V. Figure (3-b) shows the relation between Id and Vd for different values of Vg (-1.1, -2.2, and -3.3) V. It is observed that the current grew linearly with expanding gate voltage until it reaches saturation region. The highest current obtained is -0.335 mA at Vd= -3.35 V.



(a) (b)

Figure 3: Id vs. Vd properties for varies Vg values. (a): N-MOS (b): P-MOS.
Source: Authors, (2026).

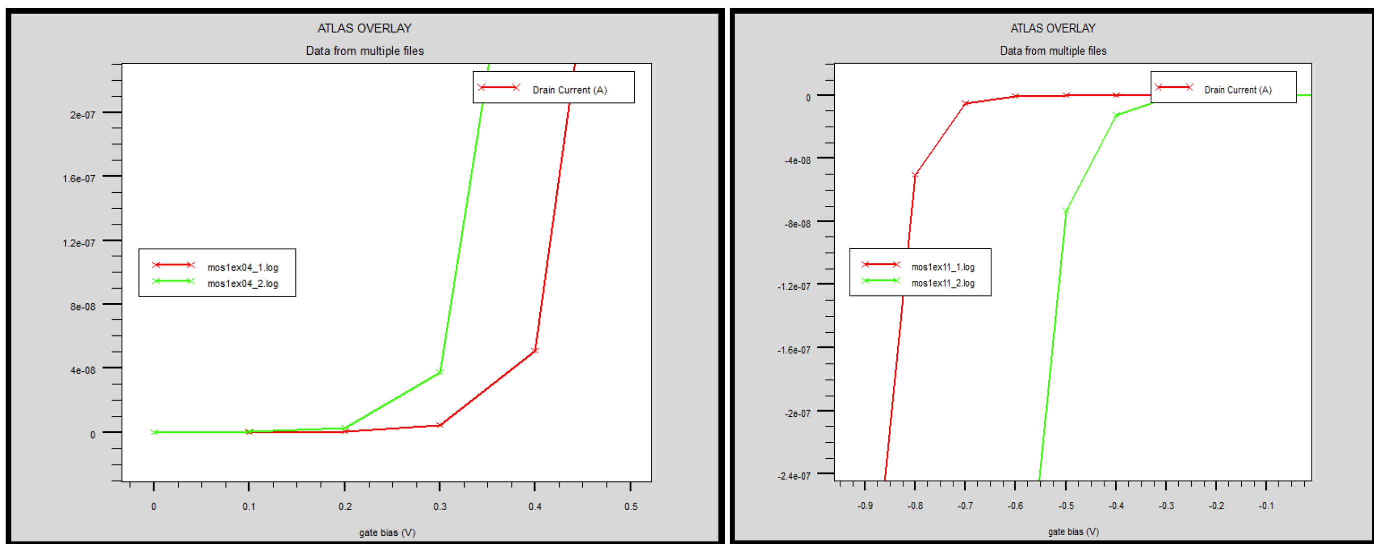
Figure (4-a) shows Id with Vg properties in the subthreshold region for N-MOS transistor. It is observed that the current exponentially proportional with Vg until reaches the subthreshold region at approximately Vg= 0.6V. Figure (4-b) shows the relation between Id and Vg in the subthreshold region for P-MOS. At Vg= 0V, the current reaches a maximum value (-12.95 A/µm). When the gate voltage is increased negatively, the current flows until it reaches a subthreshold region at Vg= -0.8V.



(a) (b)

Figure 4: Id–Vg characteristics for the subthreshold region. (a): N-MOS (b): P-MOS.
Source: Authors, (2026).

Figure (5a) shows Id verses Vg characteristics with different values of Vd for N-MOS. The red curve shows that Vt is 0.1V at Vd = 0.1V, while the green curve shows that Vt starts from 0V at Vd = 3V. It is observed that Vt reduced with increasing Vd at the same values of Id, due to DIBL. Figure (5b) shows Id Vs. Vg with different values of Vd for P-MOS. The red curve shows the behavior of normal transistor at Vd = - 0.1V, where Vt = -0.6V, while the green curve shows that Vt starts from -0.3V at Vd = -3 V also, with the same values of Id, due to DIBL.



(a) (b)

Figure 5: Id vs.Vg properties with varies values of Vd (a): N-MOS (b): P-MOS.
Source: Authors, (2026).

V. CONCLUSIONS

This is a comprehensive study Performance Valuation of Electrical Characteristics for N-MOS and P-MOS using silvaco software. The simulation of the device structures for N-MOS and P-MOS were performed. The Id vs. Vd properties for varies values of Vg and Id–Vg characteristics in the subthreshold region were studied for both transistors. Also, Id–Vg characteristics with DIBL curves were investigated for both transistors. It is concluded that N-MOS Relies on electrons as the majority charge carriers, while P-MOS Relies on holes as the main charge carriers, so N-MOS current pass from the drain to the source, while P-MOS Current pass from the source to the drain. Therefore N-MOS transistors characterized by higher performance speed due to their high electron mobility, while P-MOS transistors are easier to integrate and complement the operation of N-MOS. This makes their combination essential for achieving energy efficiency and high performance in modern integrated circuits, as achieved in C-MOS circuits, so C-MOS circuits can be designed as a EEPROM cells.

VI. AUTHOR'S CONTRIBUTION

Conceptualization: Zahra R. Mahmood, Amir M. Nory and Omar I. Alsaif.
Methodology: Amir M. Nory and Omar I. Alsaif.
Investigation: Zahra R. Mahmood, Amir M. Nory and Omar I. Alsaif.
Discussion of results: Zahra R. Mahmood, Amir M. Nory and Omar I. Alsaif.
Writing – Original Draft: Omar I. Alsaif.
Writing – Review and Editing: Zahra R. Mahmood and Omar I. Alsaif.
Resources: Zahra R. Mahmood, Amir M. Nory and Omar I. Alsaif.
Supervision: Zahra R. Mahmood, Amir M. Nory and Omar I. Alsaif.
Approval of the final text: Zahra R. Mahmood, Amir M. Nory and Omar I. Alsaif.

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