



HIGH-QUALITY POWER OF THE PACKED U-CELL 5 INVERTER USING PID AND FUZZY LOGIC CONTROL

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ABSTRACT

This research investigates the performance of five- and seven-cell packed U-Cell (PUC) inverters, highlighting their advantages in reducing harmonic distortion and improving system performance, particularly when used with low-rated filters and fewer components, compared to traditional inverters such as neutral-point clamped, cascaded H-bridge, and flying capacitor inverters. Both inverters employ a sinusoidal PWM method (Pulse Width Modulation technique). The study evaluates the effectiveness of the PUC 7 and PUC 5 inverters, emphasizing their structural differences. The PUC 7 inverter exhibits increased complexity due to the inclusion of numerous sensors and control systems that regulate the capacitor-side voltage, maintaining it at approximately one-third of the input DC voltage to ensure proper voltage balancing. This inverter faces challenges in voltage balancing and requires precise sensor measurements. In contrast, the PUC 5 inverter operates without these issues, utilizing sensorless technology that eliminates the need for voltage balancing, making it a more straightforward and more cost-effective alternative. This study also investigates the improvement of total harmonic distortion (THD) in the PUC 5 inverter through the application of fuzzy logic control and PID controllers. These control strategies aim to reduce THD and improve overall system performance. The effectiveness of the proposed methods is validated through simulations, which demonstrate the advantages of the PUC 5 inverter in terms of simplicity, performance, and reduced harmonic distortion, compared to the more complex PUC 7 inverter. The results provide valuable insights for selecting the optimal inverter configuration in applications where mitigating harmonic distortion is critical.



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I. INTRODUCTION

In recent years, A significant increase in the demand for renewable electricity was observed in 2024. Renewable energy sources accounted for 80% of the global increase in power generation, with over 700 GW of new capacity installed. Solar photovoltaic systems accounted for the predominant portion of this growth. In 2024, clean energy sources, comprising renewables and nuclear power, reached a record-high proportion of 40.9% of total global electricity generation. In the Stated Policies Scenario (STEPS), the IEA forecasts an average annual increase of 789 GW in renewable capacity until 2030, with solar photovoltaic technology representing more than 70% of this expansion.

The analysis predicts that renewable energy sources will surpass coal in electricity output for the first time in over a century, also improved, thanks to developments in power electronics. both the cost efficiency and performance of RE systems. Given the escalating global energy demand and the urgency of climate change mitigation, the demand for clean and sustainable energy sources is expected to sustain this upward trajectory [1]. The process of energy harvesting from renewable sources heavily relies on DC/AC power converters. They are crucial elements in facilitating the efficient integration of renewable energy. Optimizing the energy output from these sources into the grid. They significantly affect the reliability, cost-effectiveness, and efficiency of these systems. However, conventional two-level converters are frequently unsuitable for the applications of high-power and medium-power driven by the voltage constraints of commercially available semiconductor power devices.

When the voltage requirements of an application exceed the capacity of available power devices, series-connected switches are used in these converters. Unfortunately, this approach leads to the challenge of dynamic voltage imbalance among switching devices, which refers to the uneven distribution of voltage across the switches due to their series connection, leading to potential performance and reliability issues [2]. The multilevel converter (MLC) concept was introduced to address this issue [3],[4]. Compared to traditional two-level converters, MLCs offer several advantages, utilizing a configuration of power devices and DC sources to produce a staircase-shaped output voltage waveform. Multilevel converters have become the solution for high-power and medium-power applications due to their unique advantages. [3], [5]. Furthermore, MLCs are progressively utilized in low-voltage/power applications to address the constraints posed by two-level converters, such as high switching frequency requirements and electromagnetic interference [6], [7]. In low-voltage applications, MLCs provide a compact and efficient solution that optimizes power density and space limitations.

They minimize the system's size and weight, especially for components such as filtering and cooling systems, while achieving the desired power output by generating multiple voltage levels. This compact and efficient nature of MLCs gives us hope for a future where renewable energy systems can be more integrated and widespread [8]. Since the introduction of the MLC concept, several topologies have been developed, with many of them now being established technologies in the industry for various applications. MLC innovation began in the 1970s with the cascaded H-bridge converter, a topology that uses a series of H-bridge cells to achieve the desired output voltage [9]. This was followed by the neutral-point-clamped converter in the 1980s, which uses a set of capacitors to introduce extra voltage levels and reduce the stress on the power devices [10]. The flying capacitor converter, introduced in the 1990s, is a topology that uses a set of flying capacitors to provide the levels of the additional voltage, thereby reducing the voltage stress on the power devices [11]. These three converters are considered conventional topologies and form the foundation for more recent innovations in the field.

This table presents the THD of the flying capacitor, cascaded H-bridge, and neutral point clamped inverters [12].

Table 1: The evaluation of total harmonic distortion is conducted for NPC, FC, and CHB.

Inverters	Total harmonic distortion voltage in %
Three-level single-phase CHB, FC, and NPC inverters	58,4
Three-level three-phase CHB, FC, and NPC inverters	37,4
Five-level three-phase CHB, FC, and NPC inverters	17,2

Source: Authors, (2026).

With a lower total harmonic distortion (THD), improved efficiency, and a lower component count, PUC inverters stand out from other inverter types such as flying capacitor, diode-clamped, cascaded, and hybrid inverters. These inverters are capable of handling two types of conversion: DC-AC and AC-DC. For low-frequency operations, the PUC inverter features two additional switches that alternate between positive and negative voltage sequences, utilizing one capacitor and two high-performance switches. The result is an inverter design that is both simple and very efficient. The packed U-cell seven was initially introduced; however, its integration into industries is hindered by some limitations, rendering it less attractive despite its adequate performance level. The PUC5-level inverter addresses all these problems through efficient control operation and simplified capacitor voltage balancing. The balancing of the capacitor voltage must sustain 50% of the source voltage to produce five levels. The controller is designed for optimal performance and is resilient for seamless operation in the event of uncertainties on either the power source or load interfaces of the PUC5 design. The PUC5 inverter's unique ability to address multi-objective control challenges makes it a versatile solution for various applications. There exists an inverse relationship between capacitance and frequency that is directly contingent upon the dimensions of the capacitor. The proposed method is used to regulate the voltage, which directly affects the dimensions of the capacitor in the Packed u cell five inverter [13].

Section two elaborates on the flowchart of the suggested methodology in a step-by-step manner, providing a comprehensive understanding of the process. Section three delineates the control design, operational technique, and outcomes of the packed U-Cell 7 inverter, ensuring you are fully informed about its performance. Section four presents the control switching technique, the construction of the self-balancing voltage controller, the operational procedure, and the simulation results, providing a comprehensive overview of the inverter's operation. Section five presents a cost-saving analysis, and Section six offers a comparative analysis of both inverters based on control complexity and the components utilized [13]. In the concluding section of this paper, we apply PID and fuzzy logic control techniques to the Packed U-Cell 5 inverter to minimise total harmonic distortion (THD) effectively. These sophisticated control techniques are employed to enhance the inverter's performance, ensuring more efficient operation with reduced harmonic distortion. The outcomes derived from this implementation are subsequently compared with those of conventional multilevel inverters, emphasizing the enhanced efficiency and harmonic mitigation achieved using the proposed control methodologies. This comparison aims to illustrate the potential benefits of employing PID and fuzzy logic control to enhance the performance of modern inverter systems.

II. THEORETICAL REFERENCE

II.1 IMPLEMENTATION OF PACKED U CELL FIVE INVERTER

The PUC5 inverter presents an innovative working mode. This section examines the five-level inverter proposed by the PUC for seven levels, which operates effectively in both grid-connected and stand-alone modes while ensuring dependable and resilient dynamic performance [14].

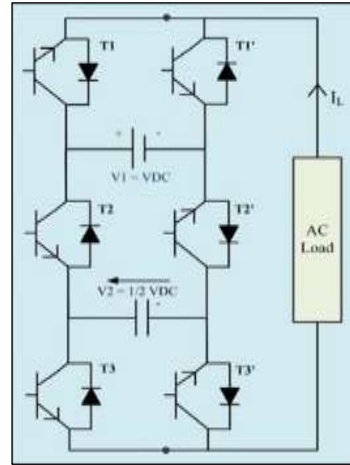


Figure 2: The 1circuit of the Packed U-Cell 5.
Source: Authors, (2026).

The structure of the 5-level PUC inverter, depicted in Figure 2, achieves sensor-less voltage regulation by utilizing redundant switching states. The controller raises the capacitor voltage to 50% of the DC source voltage, producing five-level voltages with reduced harmonic distortion. This inverter has six switches, one capacitor, and a single DC source [15]. The PUC5 inverter features a single-phase architecture, incorporating all switching states and functioning through an advanced switching technique facilitated by a sensor-less controller.

II.1.1 Voltage Regulation Switching Method

The five-level switching strategy utilizes four carrier waves (Cr1, Cr2, Cr3, and Cr4) in conjunction with a sinusoidal reference waveform (V_{ref}), as shown in Figure 10. The generation of firing pulses occurs through the comparison of V_{ref} with the carrier waves, utilizing switching states numbered 1, 2, 3, 4, 5, 6, and 8, as detailed in Table 4. Redundant states 4 and 5 are employed to minimize switching frequency. In the scenario where V_{ref} is positive, state four yields zero output. Conversely, when V_{ref} is negative, five results in zero output are observed [16].

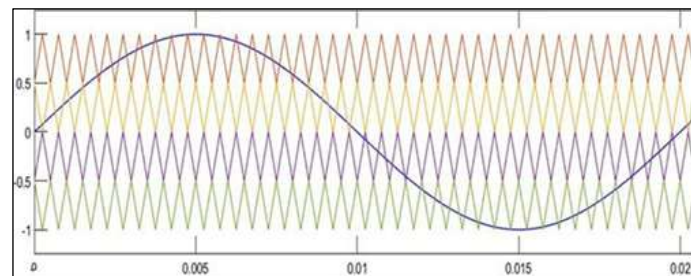


Figure 3: PUC five-level switching configuration.
Source: Authors, (2026).

II.1.2 Design of A Five-Level Self-Voltage Balancing Switching Controller For SLPUC Inverters

Figure 11 depicts the algorithm outlined, capable of maintaining the voltage across the capacitor at the specified level without the necessity of a feedback sensor. This inverter generates a consistent output voltage while operating at a low switching frequency. The proposed algorithm, when implemented on a packed u-cell five inverter, produces a 5-level voltage waveform output without requiring voltage sensors or intricate controller calculations. The voltage at the capacitor is maintained at a constant level, regardless of startup conditions or variations in load. The controller design for a seven-level inverter presents advantages by generating a seven-level output voltage with a reduced number of components. However, it introduces complexity due to the significant reliance on feedback sensors to maintain a symmetric voltage output waveform. The PUC7 inverter presents a significant challenge in terms of voltage balancing, particularly when operating at elevated switching frequencies. A new switching technique for the 5-level PUC inverter has been created to effectively address this type of problem, designed explicitly for medium power and high switching applications.

The PUC5 controller's design eliminates the need for supplementary control components, thereby reducing the complexity associated with a more elaborate controller. This controller's primary benefit lies in its straightforward design, which, when combined with elevated switching frequencies, results in superior dynamic performance. This design offers a clear advantage through its straightforward approach, which removes the necessity for voltage-balancing components. The Packed u-cell five inverter incorporates redundant switching states that are meticulously designed to align with the specifications of the PWM method, ensuring that all switching states consider the impact on the capacitor [17]. The self-voltage-balancing mechanism employs multicarrier PWM, as illustrated in Figure 11, to ensure that the capacitor voltage of the SLPUC inverter is regulated to half of the DC source amplitude. This approach circumvents the necessity for intricate controllers and removes the requirement for voltage or current sensing devices. The PUC5 inverter exhibits reduced harmonic distortion, resulting in a symmetrical output voltage waveform, while maintaining the capacitor voltage at a stable, desired level [18].

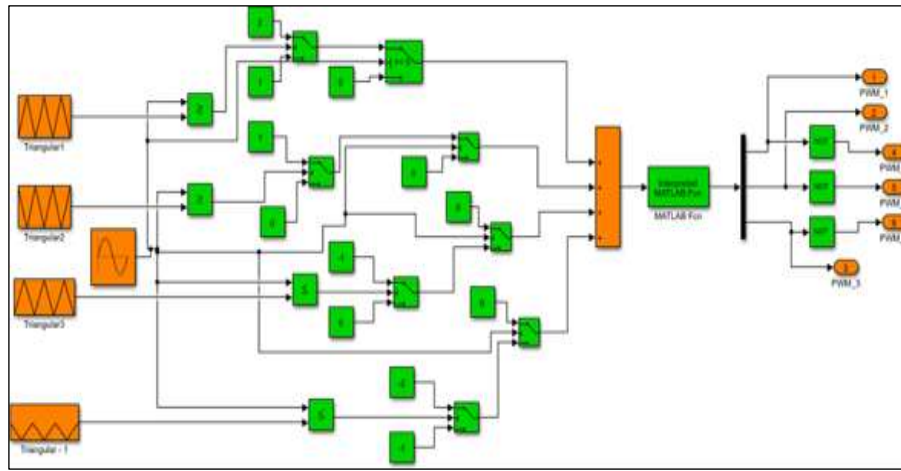


Figure 4: A Proposed Open-Loop Switching Strategy for the Packed u-Cell 5 Inverter.
Source: Authors, (2026).

II.1.3 Operation Of The Packed U-Cell Five Inverter System

Table 2 outlines the various switching states, each offering a unique pathway for current flow. The packed u-cell inverter operates as a five-level inverter by incorporating $V1 = 2V2 = 2E$, which produces a waveform featuring the voltage levels of 0, $\pm E$, and $\pm 2E$. The voltage at the capacitor ($V2$) is equivalent to 50% of the DC source voltage ($V1$). The regulation of capacitor voltage is achieved by discharging and charging the capacitor through redundant switching states, which utilize half of the DC source. A properly organized PWM scheme is crucial for controlling these excess states in the inverter [19]. Table 2 outlines the various paths created by the switching states, which are also depicted in Figure 5.

Table 2: Voltage levels generated by the packed u-cell five Inverter.

	Switch 1	Switch2	Switch3	Voltage output
State 1	1	0	0	$V1$
State 2	1	0	1	$V1-V2$
State 3	1	1	0	$V2$
State 4	1	1	1	0
State 5	0	0	0	0
State 6	0	0	1	$-V2$
State 7	0	1	0	$V2 - V1$
State 8	0	1	1	$-V1$

Source: [12].

Table 3 illustrates the inverter switching mechanism of the Packed U-Cell 5, outlining all its possible states and the various configurations that can occur during operation.

Table 3: All possible switching states of the packed u-cell 5 inverter.

	Switch 1	Switch 2	Switch 3	Output
State 1	1	0	0	$V1$
State 2	1	0	1	$V1-V2$
State 3	1	1	0	$V2$
State 4	1	1	1	0
State 5	0	0	0	0
State 6	0	0	1	$-V2$
State 7	0	1	0	$V2 - V1$
State 8	0	1	1	$-V1$

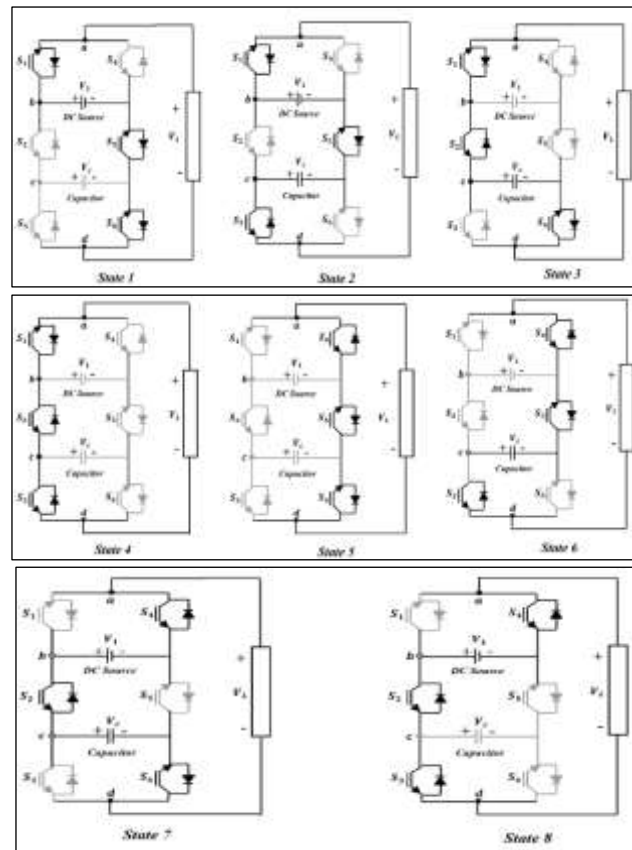
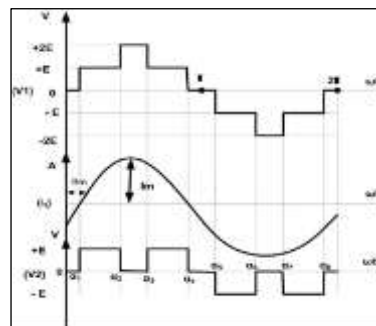
Source: [12].

Table 4 provides a detailed overview of the operational states of the capacitor, illustrating the different voltage conditions and configurations that the capacitor undergoes during the inverter's operation. Each state represents a specific phase in the inverter's functioning, helping to clarify how the capacitor behaves under various operational scenarios.

Table 4: Capacitor voltage states of PUC 5 inverter.

	Voltage of the capacitor
State 1	No Effect
State 2	Charging
State 3	Discharging
State 4	No Effect
State 5	No Effect
State 6	Discharging
State 7	Charging
State 8	No Effect

Source: [12].

Figure 5: Analysis of Existing Conduction Paths in the 5-Level PUC Inverter.
Source: [20].Figure 6: The output voltage and current waveform of a one-cycle five-level inverter.
Source: [13].

II.1.4 Analysis of The Performance of A PUC 5-Level Inverter

The PUC5 inverter undergoes testing under various load situations, including stand-alone mode and UPS applications, while considering fluctuations in load and DC supply. The inverter is employed with an RL load in this setup [20]. With a change in the DC

source voltage, the capacitor voltage precisely corresponds to the reference value ($V/2$). Figure 15 illustrates the voltage balancing waveform across the capacitor, the output voltages of the five-level inverter, and the load current, thereby demonstrating the effectiveness of the proposed sensor less voltage regulation technique incorporated into the switching pattern. The results were assessed using a MATLAB/Simulink setup.

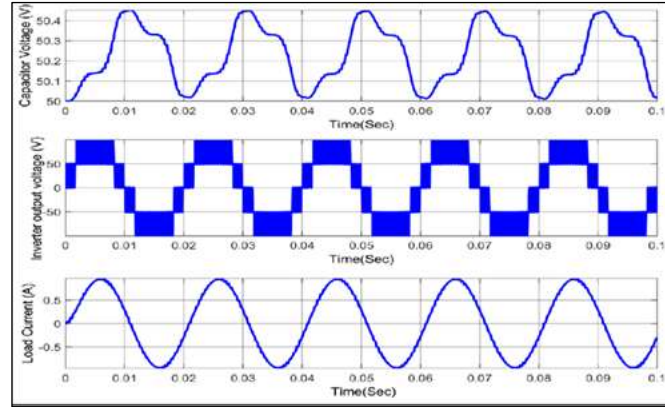


Figure 7: Representation of waveforms for: 1) Voltage across the capacitor, 2) Voltage across the load, 3) Output current.
Source: Authors, (2026).

This method does not rely on feedback sensors for the device model. The device can operate from zero voltage to any chosen amplitude, while also accommodating variations in the DC source voltage.

II.2 ECONOMIC ANALYSIS FOR COST SAVING

The cost of inverters is primarily determined by the quantity of components utilized. PUC-based inverters require a reduced number of components compared to other inverters with an equivalent number of levels. The number of levels in PUC-based inverters is dictated by the number of capacitors employed. The Flying Capacitor topology necessitates 12 switches and six capacitors to produce seven levels. In contrast, the PUC7 inverter attains the same seven levels with a 200% reduction in passive components and a 100% reduction in active components. This is achieved by decreasing the number of switches from twelve to six and reducing the number of capacitors from six to one. In the case of the flying capacitor five-level topology, eight switches and three capacitors are required.

Conversely, the packed U-cell 5 topology provides a 150% reduction in passive components. The PUC5 and PUC7 inverters exhibit increased compactness, leading to smaller and more efficient power conversion units [21]. Cost savings are evident in the decreased use of capacitors and lower voltage levels. Figure 16 depicts the correlation between voltage levels and the percentage cost of the inverter. As illustrated in Figure 17, the quantity of capacitors needed in an inverter rises with the voltage level. As a result, the expense associated with high-level inverters increases owing to the greater quantity of active and passive components [22]. The inverter cost is influenced by the number of inverter levels, which correlates with the number of capacitors, as represented by the following equation:

$$gc = (N - \log_2 (N + 1)) \cdot pc \quad (1)$$

where N = inverter level

pc = price of single capacitor

This cost percentage can be expressed by

$$gc (\%) = 100 \times (N - \log_2 (N + 1)) / (\log_2 (N + 1) - 1) \quad (2)$$

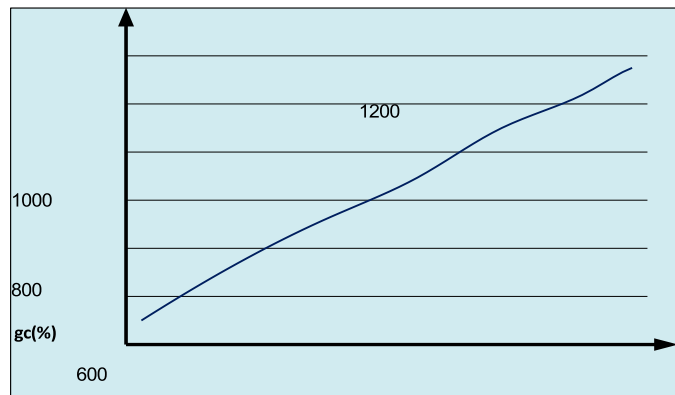


Figure 8: Percentage Cost Savings in Capacitor Usage Based on Voltage Levels
Source: Authors, (2026).

The equation for saving switches
 $gsw = (2(N - 1) - \log_2 (N + 1))$ (1)

Where $N = N_c + 1$

(3)

The power quality gain equation

$$gq = 2Nc+1 - Nc - 2 \quad (4)$$

where Nc = number of capacitors

This topology achieves a twofold increase in voltage levels compared to the flying capacitor configuration, while utilizing the same number of capacitors.

$$g_1 (\%) = 2^{Nc+1} - Nc - 2 / (\log_2 (N + 1) - 1) \quad , \quad (5)$$

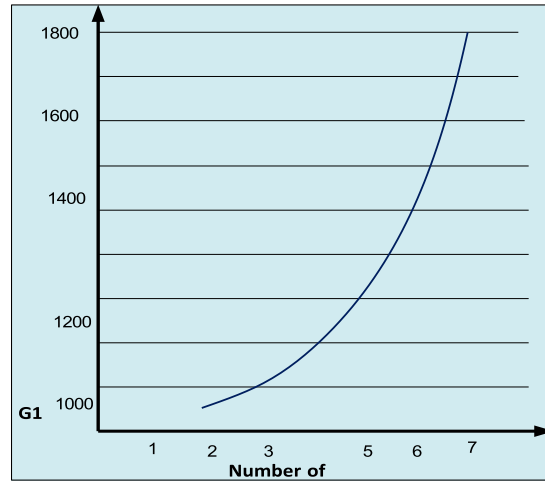


Figure 9: Enhancement of Power Quality (%) in Relation to the number of Capacitors Employed.

Source: [4].

III. RESULTS AND SIMULATION

Multilevel inverters are simulated using MATLAB/Simulink to verify PWM's performance.

Table 5: Parameters of simulation for FC, NPC, and CHB multilevel inverters

parameters	value
Flying Capacitor	1/3e-6 F
Resistance	10 Ω
DC-link-voltage	100 V

Source: Authors, (2026).

The PID parameters were determined using the Ziegler-Nichols method, beginning with initial values derived from the system's preliminary response. The values for K_p (proportional), K_i (integral), and K_d (derivative) were subsequently modified using a trial-and-error approach. The values were adjusted incrementally to achieve the optimal system response, resulting in reduced errors and enhanced system stability. Furthermore, the performance of the parameters was validated through computer simulations conducted under a range of conditions.

Table 6: Simulation parameters for PUC5 inverter

parameters	value
K_p	0.21444
K_d	0.07058
K_i	0.15779
L	250e-3 H
DC-link-voltage	100 V
R	0.1 K Ω
C	3500e-6 F

Source: Authors, (2026).

The simulation model of the packed u-cell 5 Inverter is illustrated in Figure 10, which encompasses the inverter's configuration, components, and control mechanism used for analyzing the system's performance.

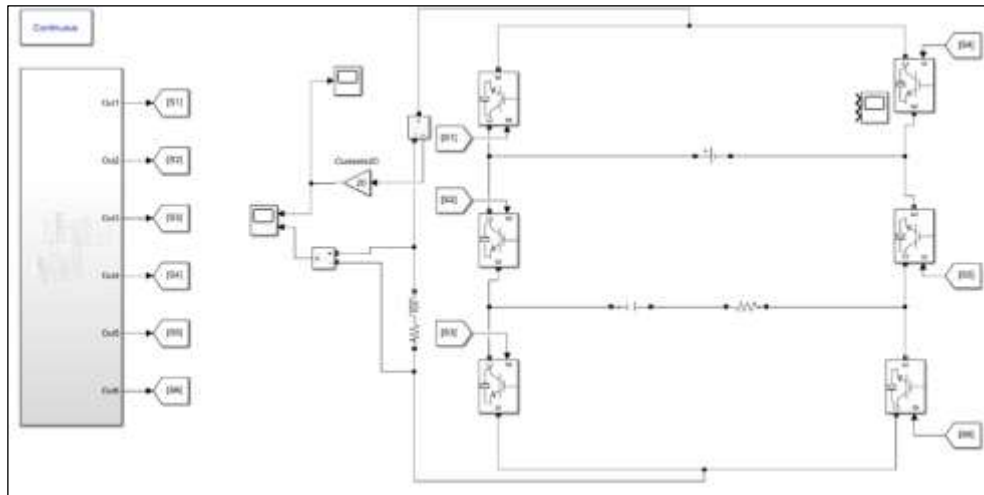


Figure.10: The model of the packed u-cell 5 inverter

Source: Authors, (2026).

Figure 11: illustrates the output voltage of the Packed U-Cell Inverter with PWM control, demonstrating typical switching behavior.

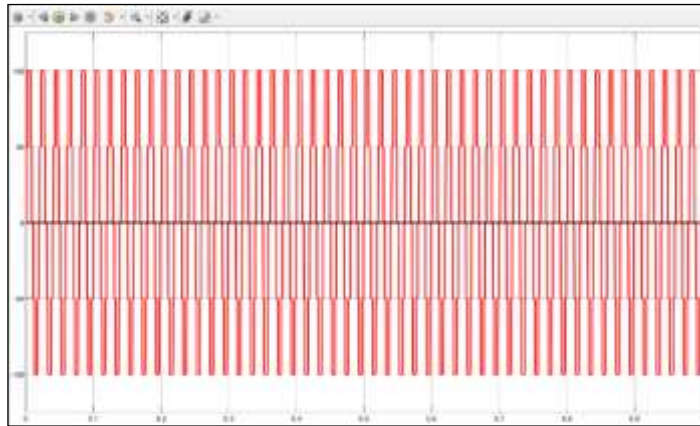


Figure 11: Output Voltage Waveform of the Packed U-Cell Inverter with Pulse Width Modulation (PWM) Control

Source: Authors, (2026).

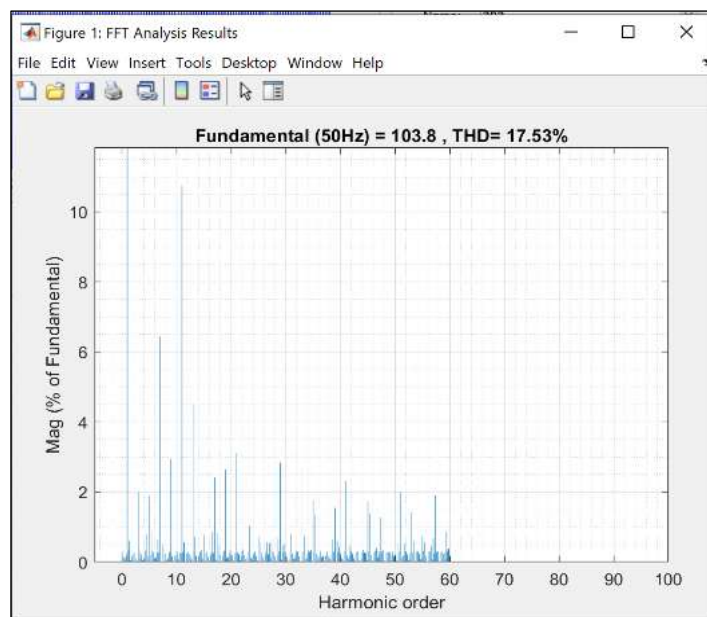


Figure 12: FFT Analysis of the Output Voltage of the PUC5 Inverter

Source: Authors, (2026).

Figure 13: illustrates the output voltage of the Packed U-Cell Inverter regulated by PID control, demonstrating a stabilised response with diminished oscillations.

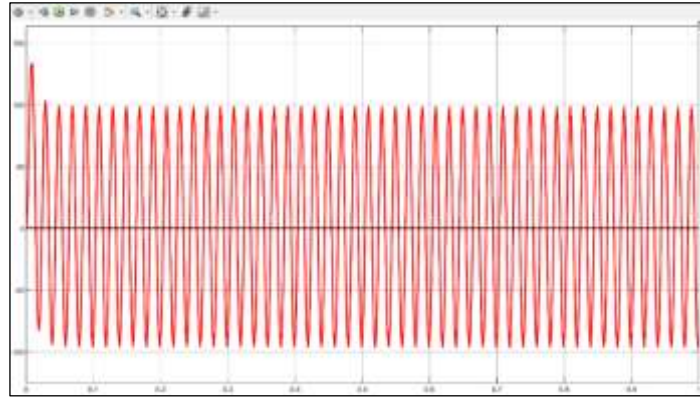


Figure 13: Output Voltage Waveform of the Packed U-Cell Inverter with PID Control.
Source: Authors, (2026).

Figure. 14: demonstrates a reduction in THD from 17.53, as seen in Figure. 12, to 1.73 after implementing the PID.

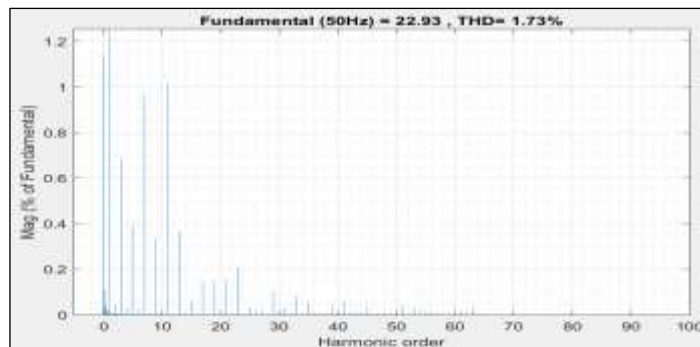


Figure.14: FFT Analysis of the Output Voltage of the packed U cell 5 Inverter with PID Control.
Source: Authors, (2026).

The figure illustrates the Output voltage of the Packed U-Cell Inverter governed by Fuzzy Logic, exhibiting seamless regulation and negligible distortion.

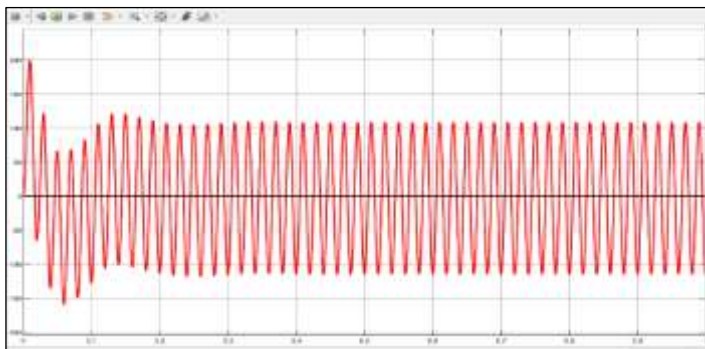


Figure 15 Output Voltage Waveform of the Packed U-Cell Inverter with Fuzzy Logic Control
Source: Authors, (2026).

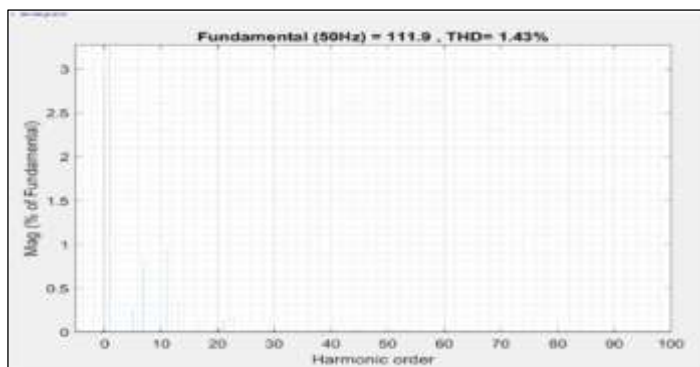


Figure 16: FFT Analysis of the Output Voltage of the packed U cell 5 Inverter with Fuzzy logic control.
Table 7 presents the Total harmonic distortion of the packed u-cell five inverter using PID and Fuzzy logic control.
Source: Authors, (2026).

Table 7: Total harmonic distortion of the PUC5 inverter using PID and Fuzzy logic control

Inverters	Total harmonic distortion voltage in %
Packed U-cell 5 inverter	17,5
Packed U-cell 5 with PID controller	1,7
Packed U-cell 5 with Fuzzy logic control	1.4

Source: Authors, (2026).

IV. RESULTS AND DISCUSSIONS

The table shows the THD values for three different Packed U-Cell 5 Inverter configurations. Applying different control systems significantly improves harmonic performance, according to the results. The amount of distortion in the waveform of the output voltage is indicated by the THD (Total Harmonic Distortion) values, which are displayed as percentages.

17 % total harmonic distortion in a packed U-cell five-inverter: Without any additional control mechanism, the Packed U-cell 5 Inverter shows a noteworthy THD value of 17.5%. This indicates that the output voltage exhibits significant harmonic distortion, which is a common issue in inverters lacking effective control systems. Increased system losses, component overheating, and potential interference with linked electrical devices are some of the negative impacts that can arise from a high total harmonic distortion (THD). The inverter is ineffective at producing clean power because the waveform is significantly distorted, meaning it deviates significantly from a perfect sinusoidal shape.

Using a packed U-cell 5 inverter with a PID controller and 1.7% total harmonic distortion installed:

Total Harmonic Distortion (THD) drops to 1.7% after using the PID (Proportional-Integral-Derivative) controller, which is a significant improvement over the unmanaged inverter. By adjusting the control variables in response to the error signal, the PID controller reduces output voltage fluctuations and harmonics. By reducing harmonic distortion, the PID controller produces a more sinusoidal waveform in the output, as shown above. With a total harmonic distortion (THD) of just 1.7%, the system is running much more efficiently. This is because the inverter can now provide power with less harmonic content, which reduces energy losses and improves the quality of the electrical power supplied to the load.

Using a packed U-cell 5 inverter with Fuzzy Logic Control and a 1.4% THD:

When compared to the PID-controlled inverter, the Fuzzy Logic Controller (FLC) achieves a Total Harmonic Distortion (THD) of as low as 1.4%. System components, such as inverters, are susceptible to unpredictable and nonlinear operating conditions; Fuzzy Logic Control is well-suited to handle these issues. As a result, the system's real-time behaviour can inform a more flexible control mechanism that adjusts settings accordingly. Fuzzy Logic Control is a suitable alternative to high-performance inverters, as it effectively reduces harmonics, as demonstrated by the 1.4% THD result. It enhances system stability and optimises the output waveform, resulting in reduced distortion and improved overall efficiency compared to conventional approaches. In conclusion, the results indicate that the Total Harmonic Distortion (THD) in the Packed U-Cell 5 Inverter's output can be significantly reduced by employing advanced control techniques, such as PID and Fuzzy Logic. At the same time, the PID controller does a good job of lowering harmonics, Fuzzy Logic Control shines, producing a cleaner and more stable output voltage by reaching the lowest THD value. For inverters to function optimally and deliver improved power, it is crucial to select the appropriate control approach. This is especially true for applications that require high efficiency with little harmonic distortion.

V. CONCLUSIONS

The designs of flying-capacitor, cascaded H-bridge, and neutral-point-clamped inverters require the incorporation of additional diodes and capacitors, which consequently increases the complexity of the system. To address these challenges, we explored the packed U-cell inverter, which provides a more efficient solution by minimizing the number of diodes and capacitors, while maintaining low Total Harmonic Distortion (THD) and reduced voltage levels. Specifically, the study focused on the Packed U-Cell 5 inverter, which, according to previous research, offers higher efficiency than the Packed U-Cell 7 despite having fewer components. Testing with a PID controller resulted in a THD of 1.7, and the application of fuzzy logic control further enhanced performance, achieving a THD of 1.4 while demonstrating efficient operation at high power levels. These findings underscore the potential of the Packed U-Cell 5 inverter in achieving a more cost-effective and efficient solution for power conversion systems.

VI. AUTHOR'S CONTRIBUTION

Conceptualization: Hakim Kadri, Abdelhalim Tlemcani And Nouredine Henini.

Methodology: Hakim Kadri, Abdelhalim Tlemcani And Nouredine Henini.

Investigation: Hakim Kadri, Abdelhalim Tlemcani and Nouredine Henini.

Discussion of results: Hakim Kadri, Abdelhalim Tlemcani And Nouredine Henini.

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Approval of the final text: Hakim Kadri, Abdelhalim Tlemcani and Nouredine Henini.

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VIII. REFERENCES

- [1] International Energy Agency, “Renewables 2024 – Executive Summary,” 2024.
- [2] A. Lunardi, L. Lourenco, E. Munkhchuluun e A. Sguarezi Filho, “Grid-Connected Power Converters: An Overview of Control Strategies for Renewable Energy,” *Energies*, vol. 15, p. 4151, November 2022.
- [3] M. basha, K. Meena e G. Prasad, “A review on multilevel inverters for power quality improvement,” *International Journal of Electrical Power & Energy Systems*, vol. 55, p. 338–349, 2014.
- [4] S. Yuvaraj e R. Karthikeyan, “Design and Optimization of Multilevel Inverters for Enhanced Power Quality in Renewable Energy Systems,” em *E3S Web of Conferences*, 2024.
- [5] A. Barnawi, A. Alfifi, Z. El-Barbary, S. Alqahtani e I. Shaik, “Review of Multilevel Inverter for High-Power Applications,” *Frontiers in Engineering and Built Environment*, vol. 4, n° 7, october 2023.
- [6] P. Grbovic, F. Crescimbin, A. Lidozzi e A. Solero, “Multi-level converters for low voltage high current applications: Issues, challenges, and limitations,” em *16th International Power Electronics and Motion Control Conference*, 2014.
- [7] M. Madi e G. Bellmunt, “EMI Levels Associated With MMC Capacitors Voltage Balancing and Their Impact on Electromagnetic Interference,” 2021.
- [8] A. Benevieri, S. Cosso, A. Formentini, M. Marchesoni, M. Passalacqua e L. Vaccaro, “Advances and perspectives in multilevel converters: A comprehensive review,” *Electronics*, vol. 13, p. 4736, 2024.
- [9] L. Tolbert, F. Peng e T. Habetler, “Multilevel Converters for Large Electric Drives,” *IEEE Transactions on Industry Applications*, vol. 35, n° 1, p. 36–44, 1999.
- [10] H. Akagi, A. Nabae e I. Takahashi, “A New Neutral-Point-Clamped PWM Inverter,” *IEEE Transactions on Industry Applications*, Vols. %1 de %2IA-17, n° 5, p. 518–523, Sep.–Oct. 1981.
- [11] T. Meynard e H. Foch, “Multi-Cell Converters,” em *IEEE Power Electronics Specialists Conference (PESC)*, 1992.
- [12] H. Kadri, A. Tlemcani e N. Henini, “Comparison Between the Most Popular Structures of Multilevel Inverters and the Packed U Cell Structure,” *International Journal of Smart Grid*, vol. 7, n° 3, pp. 128-140, 2023.
- [13] M. Ahamad, F. Garcia e A. Afthanorhan, “Packed U Cell Seven Level and Five Level Inverter Topologies for Renewable Energy Applications,” *International Journal of Modern Electrical and Renewable Energy Systems*, vol. 9, n° 4, pp. 881-901, 2024.
- [14] H. Vahedi e K. Al-Haddad, “Sensor-Less Five-Level Packed U-Cell (PUC5) Inverter Operating in Stand-Alone and Grid-Connected Modes,” *IEEE Transactions on Industrial Informatics*, vol. 12, n° 7, pp. 2350-2358, 2016.
- [15] B. Hadmer e et al, “Sliding-mode control for five-level PUC inverter with sensor-less voltage stabilization,” *Applied Sciences*, vol. 13, n° 24, p. 13018, 2023.
- [16] J. Chen, C. Wang e J. Li, “Single-phase step-up five-level inverter with phase-shifted pulse width modulation,” *J. Power Electron.*, vol. 19, n° 1, p. 134–145, 2019.
- [17] S. Arazm, H. Vahedi e K. Al-Haddad, “Phase-shift modulation technique for 5-level packed U-cell (PUC5) inverter,” em *IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2018.
- [18] M. Siddique, S. Mekhilef, N. Shah e M. Amir, “Optimal design of a new cascaded multilevel inverter topology with reduced switch count,” *IEEE Access*, vol. 7, p. 24498–24510, 2019.
- [19] M. Siddique, S. Mekhilef, S. Padmanban, C. Kumar e M. Memon, “Single Phase Step Up Switched Capacitor Based Multilevel Inverter Topology with SHEPWM Switching Approach,” *IEEE Trans. Industry Appl.*, vol. 57, n° 3, p. 3107–3119, 2021.
- [20] B. Bose, “Power electronics and motor drives: recent progress and perspective,” *IEEE Transactions on Industrial Electronics*, vol. 56, n° 2, p. 581–588, 2009.
- [21] N. Sandeep e U. Yragatti, “Operation and control of an improved hybrid nine level inverter with reduced part count,” *IEEE Transactions on Industrial Electronics*, vol. 53, n° 6, p. 5676–5686, 2017.
- [22] M. Khenar, A. Taghvaie, J. Adabi e M. Rezanejad, “Multi level inverter with combined T type and cross connected modules,” *IET Power Electronics*, vol. 11, n° 8, p. 1407–1415, 2018.