



RESEARCH ARTICLE

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POWER QUALITY ENHANCEMENT USING SHUNT ACTIVE POWER FILTER WITH ADAPTIVE INDUCTOR STEP-UP CONVERTER

Gadupudi Lakshminarayana^{1*}, Krishna Prakash Arunachalam², Pranita Chavan³, M Pandikumar⁴

¹Department of Electrical and Electronics Engineering, VNR Vignana Jyothi Institute of Engineering & Technology, Hyderabad, India.

²Departamento de Ciencias de la Construcción, Facultad de Ciencias de la Construcción Ordenamiento Territorial, Universidad Tecnológica Metropolitana, Santiago, Chile.

³Assistant Professor, Department of Electrical and Computer Engineering, Pillai HOC College of Engineering and Technology, Rasayani, University of Mumbai, 410207, India.

⁴Associate Professor, Department of Electrical Power and Energy Conversion, Saveetha School of Engineering, SIMATS, Chennai 602105, Tamil Nadu, India.

¹<https://orcid.org/0000-0003-4204-7862> , ²<https://orcid.org/0000-0002-5151-2474> ,

³<https://orcid.org/0009-0003-4016-6742> , ⁴<https://orcid.org/0000-0002-6013-1892>

E-mail: *lakshminarayana_g@vnrvjiet.in, k.prakash@utem.cl, pranitapramod44@gmail.com, pandikumarm.sse@saveetha.com.

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ABSTRACT

At present years, Power Quality (PQ) issues are considered as the major concern in power distribution systems. These PQ issues are mostly caused because of the disturbance due to the non-linear loads. PQ issues generally comprise of harmonics which is highly important to mitigate beside with compensation of reactive power. This work develops the Shunt Active Power Filter (SAPF) is the better option to diminish harmonic contamination and its performance is based on the control algorithm. The reduced switch 17 level Multi Level Inverter (MLI) is managed by a hysteresis current based PWM generator, introduces compensation currents via the SAPF to alleviate the harmonics and enhance quality of power at the Point of Common Coupling (PCC). Furthermore, to provide requisite power supply, Renewable Energy Resources (RES) based Photovoltaic (PV) system is utilized. To further boost the PV power production, an Adaptive Inductor Step-Up Converter (AISC) is deployed which enables to obtain higher level output voltage with increased voltage gain. In addition to this, Fennec Fox optimization based Artificial Neural Network (FFO-ANN)-Maximum Power Point Tracking (MPPT) strategy is employed to increase the PV power extraction process along with accurate and precise monitoring of MPP. Therefore, the developed system enables to attain improved PQ with reduced harmonics and stabilized voltage level at PCC. The implemented research is validated using MATLAB/Simulink tool and the acquired outcomes demonstrates the effective system performance, thereby, providing enhanced PQ with reduced losses.



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I. INTRODUCTION

The growing demands on non-linear loads in power distribution system led to various PQ issues [1]. Significantly, the increased usage of power electronic system over the past few years have consecutively raised the amount of non-linear loads that takes up a non-sinusoidal current from the distributed network [2-5]. Generally, this current is termed as the harmonic current, which enhances the stress in power distribution system by producing significantly higher harmonic voltage drop all over the impedance of the power network [6-8]. These issues produce huge loss to the end users as well as the distribution network [9] [10]. Therefore, proper mitigation and rectification approaches are considered essential to solve these problems [11]. For this purpose, the Active and Passive Filter are regarded as one of the best crucial solutions which removes the current and voltage harmonics within the power distribution system. To be specific Passive Filters enables to mitigate PQ issues by minimizing the harmonics while enhancing the voltage stability [12] [13].

Passive filters like low-pass filter, etc are developed to rectify high and low frequency harmonics, however, Passive filters struggles with certain drawbacks including fixed compensation which they cannot handle dynamic load conditions, these filters require large number of components such as inductor and capacitors, thereby increasing the filter overall filter size and weight with reduced harmonics rectification process [14] [15]. Therefore, Active Power Filters (APF) are considered highly for PQ improvement applications over passive filters. Considering various APF like Series Active Power Filters (SAPF) [16] [17] and Hybrid Active Power Filters (HAPF) [18] enables highly efficient performance with optimum PQ improvement while reducing voltage and current disturbances. However, these approaches are prone to increased complexity with increased losses. Henceforth, SAPF technique is deployed to compensate current harmonics and reactive power along with effective removal of current harmonics while increasing PQ, reactive power compensation by enabling rapid dynamic response rate.

Furthermore, to provide enhanced, consistent and sustainable power supply, RES based PV is highly used. However, PV initially produces low level output voltages which makes it essential to utilize appropriate power converters to boost the PV power production process [19]. Conventional converters such as Boost [20], SEPIC [21], Cuk [22] and Interleaved Boost converters [23] provides enhanced boosting and regulation of PV power generation process with improved voltage gain. Despite this, these converters depicts certain issues such as increased duty cycle, complexity, higher component stress and increased cost of implementation. Therefore, here AISC is utilized which offers increased voltage gain with reduced ripples and switching losses, improving the total efficacy of the PV system producing higher level output voltage. In addition to this, for extracting highest power from PV, Optimized MPPT approaches are deployed which also enables to track and monitor MPP [24]. Existing MPPT approaches such as Whale Optimization Algorithm (WOA) - Model reference

Adaptive Control (MRAC) [25] which provides enhanced tracking efficiency with increased convergence speed, but this method struggles with increased computational complexity and cost of implementation. Significantly, in [26] the authors utilized Novel Adaptive Step (NAS)-Incremental Conductance (INC) based MPPT technique which allows rapid convergence speed while achieving enhanced tracking of MPP with reduced deviations even under varying environmental circumstances. However, NAS-INC suffers from instability and unreliability due to tracking delays. Likewise, PSO-Machine Learning (ML) based MPPT method is deployed for attaining improved tracking of MPP with increased convergence speed, in spite this, PSO-ML topology struggles with increased computational complexity and higher sensitivity to parameter tuning and this method cannot handle varying environmental conditions. Therefore, here FFO-ANN based MPPT technique is deployed which offers enhanced tracking efficiency with increased convergence speed and highest power tracking from PV. Henceforth, the overall proposed system offers improved PQ mitigation while reducing current and voltage harmonics. The objectives are,

- To implement SAPF to improve the PQ by attaining reduced harmonic and increased reactive power compensation.
- To integrate RES based PV system to provide sustainable power supply to meet the desired power requirements of the system which in turn rises the power distribution system's reliability.
- To deploy an AISC converter to attain highly regulated PV power production with increased voltage gain with reduced power losses and ripples.
- To utilize FFO-ANN based MPPT technique for obtaining highest power extraction from PV along with accurate and precise tracking of MPP with increased convergence speed.

II. PROPOSED METHODOLOGY

Figure 1 illuminates the developed system block diagram, initially the process begins with PV which produces electricity from solar energy. However, PV in the beginning produces low level output voltage, for which AISC is deployed which regulates the PV power production by achieving higher level output voltage with increased gain and reduced losses. Later, for extracting maximum power from PV and to track MPP, FFO-ANN based MPPT technique is attached which depicts increased convergence speed with accurate MPP monitoring.

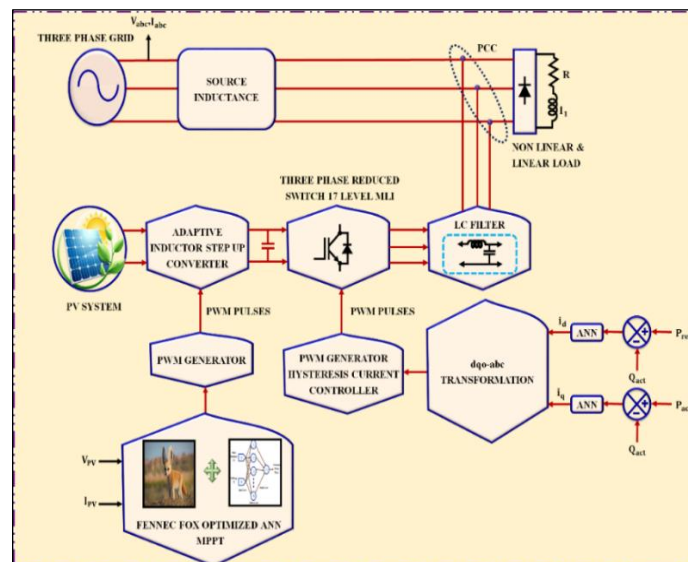


Figure 1: Proposed system block diagram.
Source: Authors, (2026).

The output attained from the converter is further controlled utilizing the PWM generator, which in turn regulates the voltage level. A reduced-switch 17-level MLI transforms the controlled DC power into AC, minimalizing harmonic distortion. The MLI is managed by a hysteresis current-based PWM generator, injects compensation currents via the SAPF to alleviate harmonics and increase power quality at the PCC. Then dq0-abc transformer is connected to PWM generator controller for converting reference and actual power. Furthermore, an ANN based control technique is utilized for producing the required reactive and active power references for assuring improved grid stability and reliability, thereby achieving enhanced power flow maintenance at the linear and non-linear load region. Before proceeding to PCC, the output is allowed to pass through LC filter which removes any unwanted interferences and harmonics. Therefore, the proposed system as a whole offers enhanced PQ improvement using shunt active power filtering technique along with integrated PV with suitable converter and MPPT approach offers consistent and sustainable power supply.

II.1 MODELLING OF SAPF

The control and power the circuit develops a SAPF, as seen in Figure 2. The necessary compensating current is synthesized by the power circuit. It uses a DC-link capacitor to store energy and maintain and control the dc voltage, along with a PWM related voltage source inverter. Additionally, to compute the instant reference compensation current, the control circuit unceasingly observes the harmonic current changes and it regulates the power circuit to exactly produce the necessary harmonic current. The methods used for harmonic extraction and current management decides the efficacy of the harmonic current compensation procedure. The flow of current in the power system is stated as below prior to the filter being linked at the PCC.

$$i_s = i_L = i_{1L} + i_H \quad (1)$$

Where i_s is current at source side, i_L is the current at load side, i_{1L} is the vital component of i_L and i_H is the harmonic component of i_L .

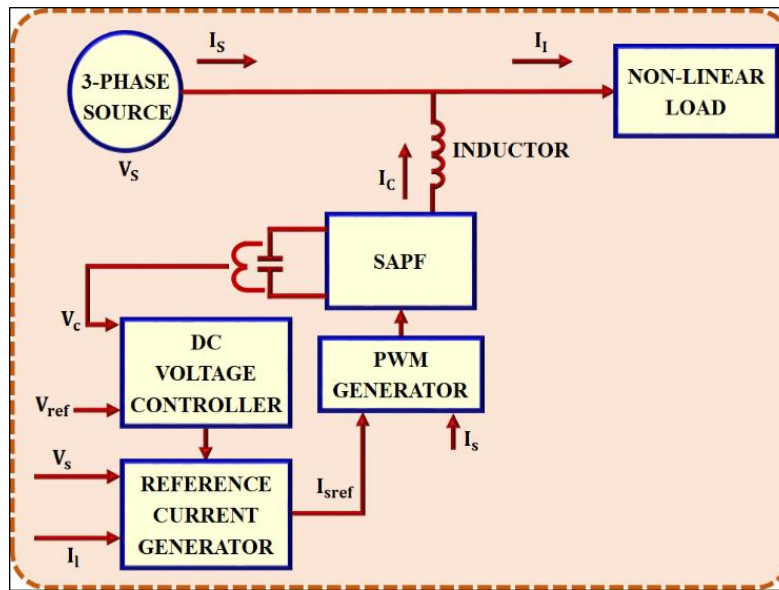


Figure 2: Structure of SAPF.

Source: Authors, (2026).

Two additional currents are then presented when the SAPF is placed at the PCC. The DC-link current (i_{dc}), which the SAPF uses to sustain the DC-link voltage (V_{dc}), at the appropriate level and the harmonic compensation current is equal in magnitude to the harmonic current however has a 180° shift. The power system's current flow is,

$$i_s = i_L = [i_{1L} + i_H] - i_c + i_{dc} \quad (2)$$

Where i_c is the injected compensation current. The produced harmonic compensation current is exactly the similar to the harmonic current generated by the nonlinear load and they terminate each other out if the voltage across the dc link capacitor is reserved at the predefined level. As a result, the expression (2) becomes,

$$i_s = i_{1L} + i_{dc} \quad (3)$$

Then, the reduced switch 17 level MLI is utilized for improving the power quality of overall system by eliminating the harmonics.

II.2 MODELLING OF THREE PHASE REDUCED SWITCH 17 LEVEL MLI

The circuit diagram for the developed MLI topology is shown in Figure 3, which is powered by a single DC source and consists of 20 switches ($S_1, \dots, S_{20}$) and four capacitors ($C_1, \dots, C_4$). The input DC source is a solar cell or battery. The voltage gain of this design is 4 times the supply voltage. In this case, 100V is the input dc voltage source. X and Y identify the load terminal, while $V_{XY}(t)$ and $I_{XY}(t)$ stand for the terminal loads' voltage and current, respectively.

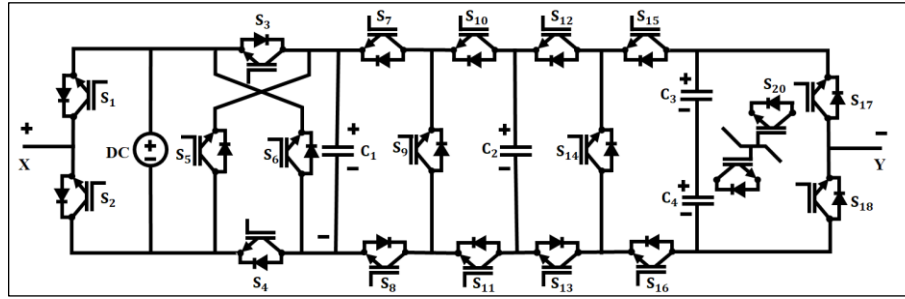


Figure 3: Structure of Reduced Switch 17 level MLI.

Source: Authors, (2026).

State 1 & State 17

In this modes, the switches $S_2, S_{12}, S_6, S_7, S_9, S_{11}, S_{14}, S_{16}$ and S_{17} are activated and the voltage on output side is +400V. The supply source is connected in string to the capacitors $C_1, \dots, C_4$, which releases their stored energy to the load via the DC voltage source.

Table 1: Switching Table of Proposed MLI.

M	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	S_{17}	S_{18}	S_{19}	S_{20}	V_0
1	0	1	0	0	0	1	1	0	1	0	1	1	0	1	0	1	1	0	0	0	400
2	0	1	0	0	0	1	1	0	1	0	1	1	0	1	0	1	0	0	1	1	350
3	0	1	1	1	0	0	1	0	1	0	1	1	0	1	0	1	1	0	0	0	300
4	0	1	1	1	0	0	1	0	1	0	1	1	0	1	0	1	0	0	1	1	250
5	0	1	1	1	0	0	1	1	0	1	1	1	1	1	0	1	1	0	0	0	200
6	0	1	1	1	0	0	1	1	0	1	1	1	1	1	0	1	0	0	1	1	150
7	0	1	1	1	0	0	1	1	0	1	0	1	1	0	1	1	1	0	0	0	100
8	0	1	1	1	0	0	1	1	0	1	1	1	1	0	1	1	0	0	1	1	50
9	0	1	1	1	0	0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	0
10	1	0	1	1	0	0	1	1	0	1	1	1	1	0	1	1	0	0	0	0	-50
11	1	0	1	1	0	0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	-100
12	1	0	1	1	0	0	1	1	0	1	1	1	1	1	1	0	0	0	1	1	-150
13	1	0	1	1	0	0	0	1	0	1	1	1	1	1	1	0	0	1	0	0	-200
14	1	0	1	1	0	0	0	1	1	1	0	0	1	1	1	0	0	0	1	1	-250
15	1	0	1	1	0	0	0	1	1	1	0	0	1	1	1	0	0	1	0	0	-300
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-350
17	1	0	0	0	1	0	0	1	1	1	0	0	1	1	1	0	0	1	0	0	-400

Source: Authors, (2026).

State 2 & State 16

The voltage on output side is +350V when the switches $S_2, S_6, S_7, S_9, S_{11}, S_{12}, S_{14}, S_{16}, S_{19}$ and S_{20} are activated. In this mode, the input supply source releases the stored energy from C_1, C_2 and C_4 that are in chain with the source.

State 3 & State 15

In this stage, the switches $S_{11}, S_2, S_{12}, S_{14}, S_{16}, S_3, S_4, S_7, S_9$ and S_{17} are on and the output voltage is +300V. The C_3, C_2 and C_4 are in line with the supply source. Therefore, the capacitors release their stored energy to the load in tandem with the DC voltage source.

State 4 & State 14

The voltage on output side is +250V when $S_{11}, S_{12}, S_{14}, S_{16}, S_{19}, S_2, S_3, S_4, S_7, S_9$ and S_{20} are activated. In this mode, the input supply source and the collected energy from C_2 and C_4 linked in sequence with the source are released to the load.

State 5 & State 13

The voltage on output side is +200V in this switching state and $S_{12}, S_{13}, S_{14}, S_7, S_8, S_{10}, S_2, S_3, S_4, S_{11}, S_{16}$ and S_{17} are activated. In this mode, C_3, C_2 and C_4 are linked in parallel to the source, liberating the stored energy to the load via the source.

State 6 & State 12

The voltage on output side is +150V when the switches $S_{10}, S_{11}, S_{13}, S_{14}, S_{16}, S_{12}, S_2, S_3, S_4, S_7, S_8, S_{19}$ and S_{20} are activated. In this mode, C_2 and C_4 are in line with the source and the energy they have stored is liberated to the load beside with the input.

Mode 7& Mode 11

In this mode, the switches $S_{10}, S_{11}, S_{12}, S_2, S_3, S_4, S_7, S_8, S_{13}, S_{15}, S_{16}$ and S_{17} are turned on and the output voltage is $+100V$. Because C_1, C_2 and C_3 are linked in parallel to the supply source during this stage, they charge up to a dc source and C_3 and C_4 up to $5V_{dc}$.

State 8 & State 10

The output voltage is $+50V$ when the switches $S_7, S_8, S_{10}, S_{11}, S_{12}, S_{13}, S_{15}, S_2, S_3, S_4, S_{16}, S_{19}$ and S_{20} are activated. Because C_2 and C_4 are connected in parallel to the source during this stage, C_1 and C_2 charge to the voltage of source, while C_3 and C_4 charge to $0.5V_{dc}$.

State 9

In this stage, $S_8, S_{10}, S_{11}, S_2, S_3, S_4, S_7, S_{15}, S_{16}, S_{12}, S_{13}$ and S_{18} have zero output voltage. C_1 and C_2 are charged to the voltage on input side, while capacitors C_3 and C_4 are charged to $5V_{dc}$. To provide the supply for the SAPF, the PV system is exploited and is discussed below.

II.3 MODELLING OF PV SYSTEM

Figure 4 represents the circuit diagram of the PV cell, which comprises of a single diode. Here, I and p indicates the output current of PV and voltage, I_L refers to the photon produced current, I_D indicates the diode current, R_s and R_{sh} implies the series and shunt resistance respectively.

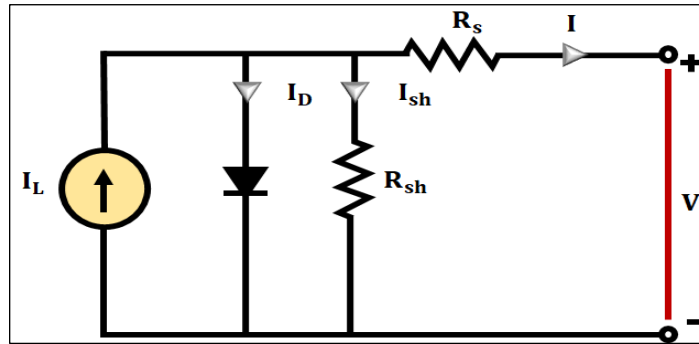


Figure 4: Equivalent circuit of the PV system.

Source: Authors, (2026).

The $I - V$ characteristics of the PV system is expressed using,

$$I = I_L - I_D - I_{SH} \quad (4)$$

$$I_D = I_0 \left(e^{\frac{q(V-IR_s)}{\alpha kT}} - 1 \right) \quad (5)$$

$$I_{SH} = \frac{V - IR_s}{R_{SH}} \quad (6)$$

Where, α and k indicates the diode quality factor and Boltzmann's constant, T and q implies the absolute temperature and charge of the electron respectively. The low voltage of PV system is enhanced by utilizing the AISC.

II.4 MODELLING OF AISC

Figure 5 shows the power circuit of a developed AISC converter that represents the AISC as an ideal transformer with a ratio of $N_1:N_2$, a magnetizing inductance of L_y and a leakage inductance of L_x . The ratio of the coupled inductor turn is therefore assumed to be $n = N_2 / N_1$. The waveform of the converter operation are also depicted in Figure 6.

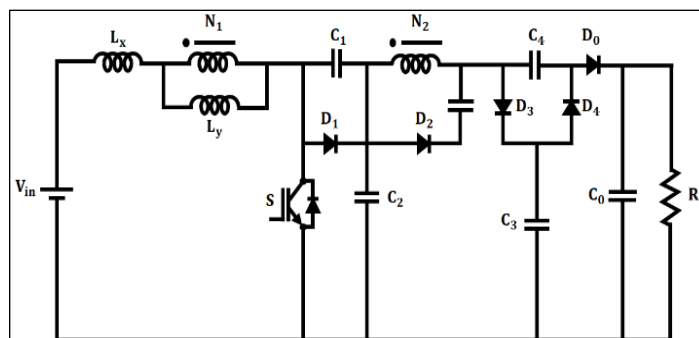


Figure 5: Circuit diagram of AISC.

Source: Authors, (2026).

Mode 1:

Diodes D_3 and D_0 are on in the first mode, and the power switch S begins to conduct. Leakage and magnetizing inductance currents rise linearly, as shown in Figure 7 (a). The second winding is used to charge capacitor C_3 . Additionally, the input voltage charges the magnetizing inductance and the load receives the energy from capacitors C_1 and C_4 . When the leakage inductance current equals the magnetizing inductance current, this stage is finished.

Mode 2:

The power switch S remains on in the second mode, D_1 , D_3 and D_0 are reverse biased, while the diodes D_2 and D_4 are active. In this mode, C_4 is charged via C_5 and the energy from the input source is passed to the magnetizing inductance, as depicted in Figure 7 (b). Additionally, the transformer's secondary side charges C_1 and the capacitor C_0 provides the load's energy. When the main switch is switched off, this mode ends. The voltage of capacitors and magnetizing inductance is expressed as,

$$V_{Lx} = V_{in} \quad (7)$$

$$V_{C1} - V_{C3} - V_{C2} = nV_{in} \quad (8)$$

$$V_{C2} + V_{C3} + V_{C4} - V_{C5} = 0 \quad (9)$$

Mode 3:

At this mode, diodes D_1 , D_2 and D_4 conduct and switch S is off, as seen in Figure 7 (c). The leaking inductor's current decreases linearly before passing through diode D_1 and activating it. In this mode, diode D_2 is used to charge capacitor C_3 . Additionally, capacitor C_5 continues to charge capacitor C_4 . Additionally, the load takes the power from the C_0 . When the magnetizing and leakage inductance currents equalize, this time stage is completed.

Mode 4:

In this mode, diodes D_1 , D_3 and D_0 are in the on-state, diodes D_2 and D_4 are blocked and switch S remains in the inactive state, as displayed in Figure 7 (d). The currents of magnetizing inductance I_{Ly} and leakage inductance I_{Lx} decrease linearly during this time period. Through diode D_1 , the leakage inductance's stored energy is demagnetized and sent to capacitor C_2 . In the meantime, energy is transferred to the load and the C_0 is charged by the V_{in} and capacitors C_1 and C_4 . This time interval ends when diode D_1 is blocked at $t = t_4$.

$$V_{Ly} = V_{in} - V_{C2} \quad (10)$$

$$V_0 = V_{C5} + V_{C4} \quad (11)$$

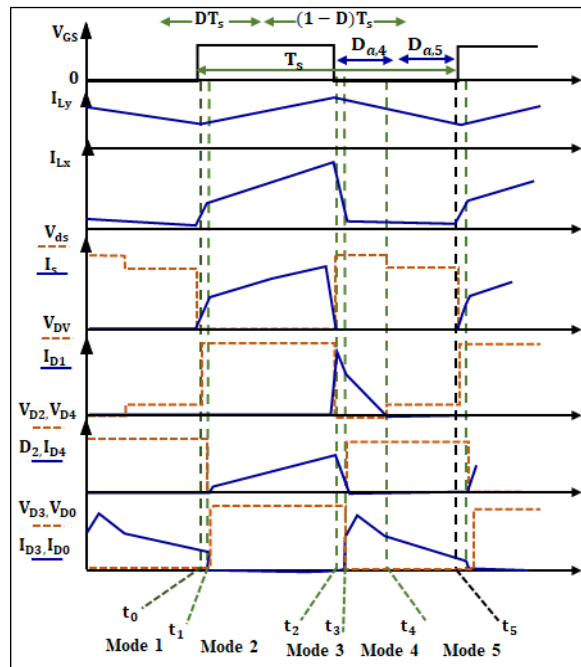


Figure 6: Waveform of AISC.

Source: Authors, (2026).

Mode 5:

In this state, diodes D_3 and D_0 are forward biased and switch S is still off. Additionally, the magnetizing and leakage inductance currents drop linearly. In this stage, the capacitor C_0 and load receive energy from V_{in} , leakage inductance and magnetizing inductance in addition to capacitors C_1 and C_4 . By turning on the main power switch once more, this time transition comes to an end and the subsequently switching period is started, as revealed in Figure 7 (e). The voltage across the magnetizing inductance is.

$$V_{Ly} = V_{in} - V_{C5} + V_{C3} + V_{C1} \quad (12)$$

The voltage across capacitor C_3 is

$$V_{C3} = nV_{C2} - nV_{in} \quad (13)$$

The following expressions are obtained in this stage,

$$V_{Lx}^{mode5} = \frac{I_{Lx}^{mode5}}{(D_{t4,5})T_s} L_x \quad (14)$$

$$I_{Lx}^{mode5} = I_{Ly} - I_{N1} \quad (15)$$

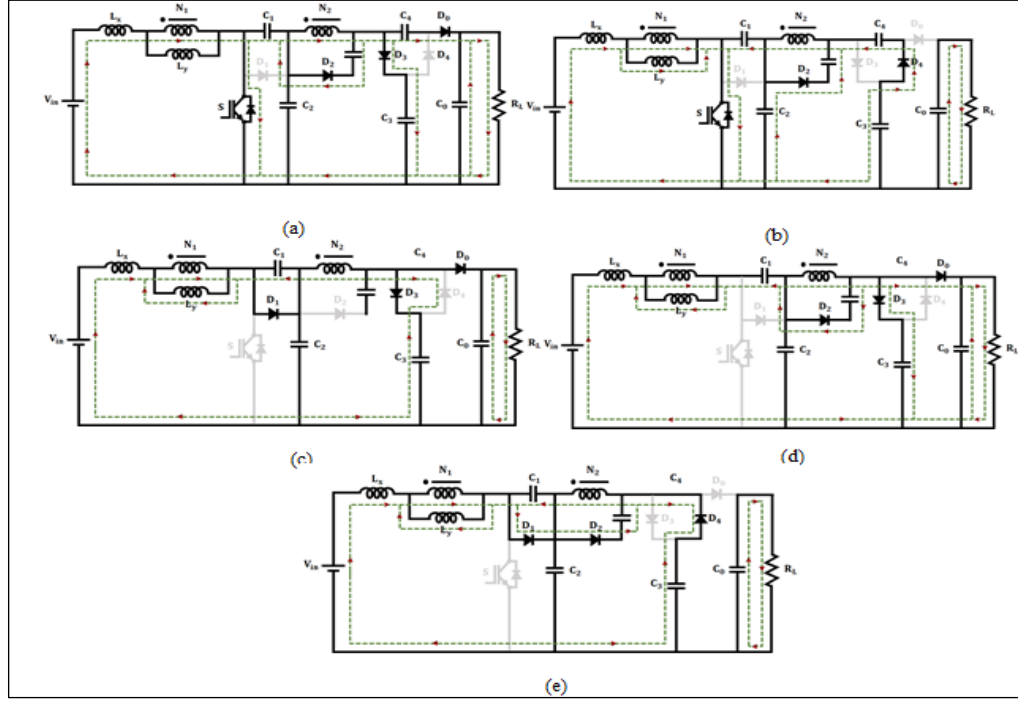


Figure 7: Stages of AISC (a) Mode 1 (b) Mode 2 (c) Mode 3 (d) Mode 4 (e) Mode 5.

Source: Authors, (2026).

The current slope of the leaking inductance is zero when the magnetizing inductance's current ripple is ignored. As a result, there is no voltage across the leaking inductance. This equation states that the switch's current is zero when it is turned on at the start of the first mode. Consequently, in zero current switching conditions, the switch is activated. The associated inductor leakage inductance is disregarded in order to streamline the converter's steady-state analysis. Additionally, switching device power losses are not considered. Because the time intervals between stages 1 and 3 are so short, only modes 2, 4, and 5 are considered in CCM analysis. Thus, by utilizing the inductor volt-second balance law for magnetising inductance is,

$$\int_0^{DT_s} V_{in} dt + \int_{DT_s}^{T_s} (V_{in} - V_{C2}) dt = 0 \quad (16)$$

The voltage across capacitor C_2 is,

$$V_{C2} = \frac{V_{in}}{1-D} \quad (17)$$

Where D is the power switch duty cycle. The voltages across capacitor C_3 is,

$$V_{C3} = \frac{nD}{1-D} V_{in} \quad (18)$$

The voltage across capacitor C_1 is,

$$V_{C1} = \frac{(n+1)}{1-D} V_{in} \quad (19)$$

The voltage across capacitor C_5 is,

$$V_{C5} = \frac{(2+n+nD)}{1-D} V_{in} \quad (20)$$

The voltage of the capacitor C_4 is,

$$V_{C4} = \frac{(n+1)}{1-D} V_{in} \quad (21)$$

The voltage gain is,

$$M_{CCM} = \frac{V_0}{V_{in}} = \frac{(3+2n+nD)}{(1-D)} \quad (22)$$

The highest power from PV system is tracked with the aid of ANN-MPPT controller and its parameters are fine-tuned by FFA algorithm.

II.5 MODELLING OF FFA-ANN MPPT CONTROLLER

The current-voltage curve of PV system, generally comprises of unique point which is known as the MPP, at these points the PV system functions with highest efficacy and generates maximum PV output power. To further maintain the PV performance while attaining maximum power output, MPPT controller techniques play a major role. Significantly, the MPPT controller controls the PV current and voltage based on the load. Here, the PV voltage is controlled using ANN, the reference voltage (V_{MPP}) in real-time depends on the solar irradiation (G) and temperature (T) respectively. ANN generally comprises of three layers, as represented in Figure 8.

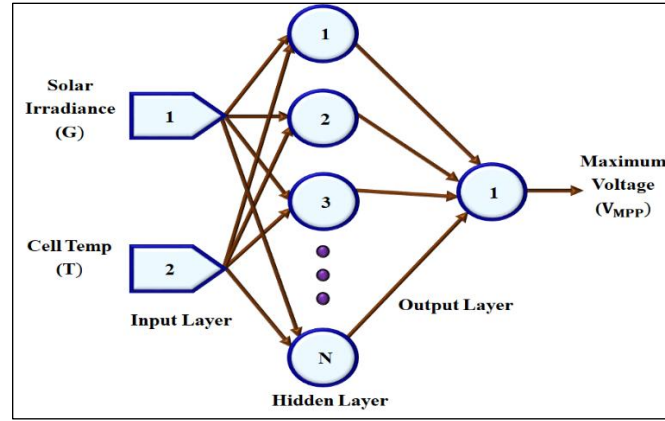


Figure 8 ANN structure for MPPT controller .
Source: Authors, (2026).

However, to further enhance the ANN-MPPT controller performance, it is essential to attain optimum tuning of the parameters, which is accomplished using FFA. The fennec fox is one among the member of the vulpes family of the foxes which is the smallest species and are also easily identified using the huge ears. These foxes are an omnivorous animal which mainly prefers lizards, small rodents, skinks, tiny insects, eggs and fruits. The fennec fox comprises of two behaviours which is strong digging ability and their capabilities to escape from predators. These two behaviours of fennec foxes are considered as highly significant strategies. On basis of these two intelligent aspects the FFA algorithm is designed and developed. The first step in FFA is initialization. FFA is a population related algorithm where each fennec fox is the search member. Significantly, in FFA, each and every fennec fox implies the solution to the optimization issue whose position in the search space represents the decision variable's values. The fennec fox vector and its corresponding population matrix is initialized using,

$$X_i : x_{i,j} = lb_j + r \cdot (ub_j - lb_j), i = 1, 2, \dots, N, j = 1, 2, \dots, m \quad (23)$$

Where, X_i represents i^{th} fennec fox, $x_{i,j}$ indicates the j^{th} dimension, N denotes the total number of fennec foxes, m implies the total number decision variable, r refers to the random number between $[0,1]$, lb_j and ub_j signifies the lower and upper bound of the j^{th} decision variable. The population matrix is represented using,

$$X = \begin{bmatrix} X_1 \\ \vdots \\ X_i \\ \vdots \\ X_N \end{bmatrix}_{N \times m} = \begin{bmatrix} x_{1,1} & \cdots & x_{1,j} & \cdots & x_{1,m} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ x_{i,1} & \cdots & x_{i,j} & \cdots & x_{i,m} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ x_{N,1} & \cdots & x_{N,j} & \cdots & x_{N,m} \end{bmatrix}_{N \times m} \quad (24)$$

Where, $X_i = (x_{i1}, x_{i2}, \dots, x_{im})$ denotes the i^{th} fennec fox within the range of N and the candidate for the j^{th} decision variable for is represented using each column $(x_{1j}, x_{2j}, \dots, x_{Nj})^T$ respectively. The candidate value attained by each of the fennec fox are positioned in the objective function's variables which are mathematically termed as,

$$F = \begin{bmatrix} F_1 \\ \vdots \\ F_i \\ \vdots \\ F_N \end{bmatrix}_{N \times 1} = \begin{bmatrix} F(X_1) \\ \vdots \\ F(X_i) \\ \vdots \\ F(X_N) \end{bmatrix}_{N \times 1} \quad (25)$$

Where, F represents the objective function's vector value, F_i indicates the objective function attained from the i^{th} fennec fox respectively. Later, the candidate with finest objective function is chosen as the optimum solution and the candidate position is updated after each iteration.

The natural behaviour of the fennec foxes are classified into two type such as Digging to find prey under the sand and evading from the predators. The fennec foxes usually hunt during the night and in solitude by using their extreme power of hearing with its large ears for detecting prey under the sand. Later, once the prey location is found, these foxes dig the sand using their feet to expose and hunt their prey. For designing the model of fennec fox during the digging process, considering the neighbourhood within a radius R across its actual position. The updating stage of FFA candidates is represented using,

$$x_{i,j}^{P1} = x_{i,j} + (2.r - 1).R_{i,j}, \quad (26)$$

$$R_{i,j} = \alpha \cdot \left(1 - \frac{t}{T}\right) \cdot x_{i,j}, \quad (27)$$

$$X_i = \begin{cases} X_i^{P1}, & F_i^{P1} < F_i, \\ X_i, & \text{else,} \end{cases} \quad (28)$$

Where, X_i^{P1} represents the new predicted position of the i^{th} fennec fox on the base of the first stage, $x_{i,j}^{P1}$ represents the j^{th} dimension, F_i^{P1} denotes the objective function, $R_{i,j}$ implies the neighbourhood radius, t refer to iteration counter, T denotes the number of total iterations and lastly, α indicates the constant respectively. Generally, fennec foxes are often attacked by predator like Pharaoh eagle-owl, hyenas and caracals. Despite this, fennec foxes always find a way to escape from these predators utilizing their incredible speed and rapid change in the movement direction. In FFA, this approach is termed as the search space's global scanning. Significantly, it improves the exploration process and also enables to escape from getting stuck in local optima. The random position of these fennec foxes are regarded as the behaviour of fennec foxes during their escape which is mathematically expressed utilizing,

$$X_i^{rand}: x_{i,j}^{rand} = x_{k,j}, k \in \{1, 2, \dots, N\}, i = 1, 2, \dots, N, \quad (29)$$

$$x_{i,j}^{P2} = \begin{cases} x_{i,j} + r \cdot (x_{i,j}^{rand} - 1 \cdot x_{i,j}), & F_i^{rand} < F_i, \\ x_{i,j} + r \cdot (x_{i,j} + r \cdot (x_{i,j} - x_{i,j}^{rand})), & \text{else} \end{cases} \quad (30)$$

$$X_i = \begin{cases} X_i^{P2}, & F_i^{P2} < F_i, \\ X_i, & \text{else} \end{cases} \quad (31)$$

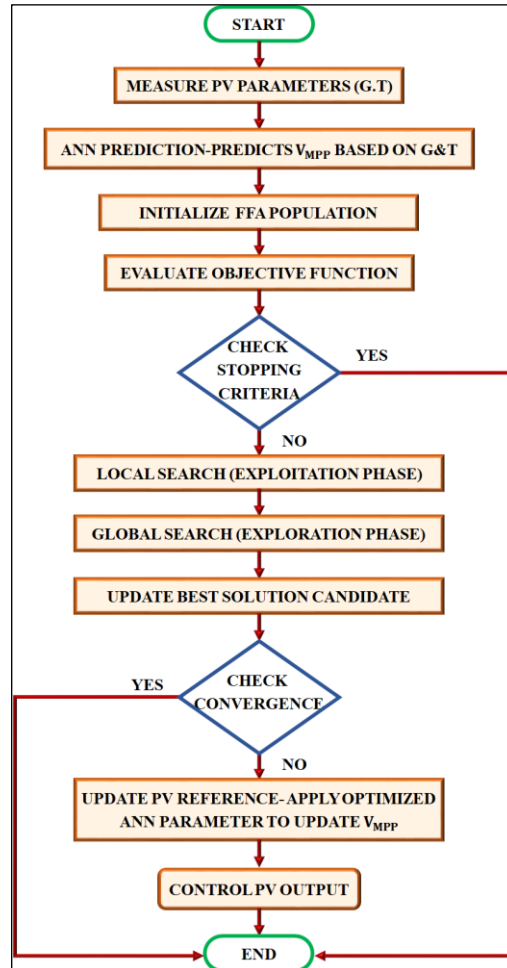


Figure 9: Flowchart of FFA-ANN MPPT Controller.
Source: Authors, (2026).

Where, X_i^{rand} denotes the target position determined for escape of the i^{th} fennec fox, $x_{i,j}^{rand}$ indicates the j^{th} dimension, F_i^{rand} depicts its objective function, X_i^{P2} refers to the new updated position of the fennec fox on the second stage's basis, $x_{i,j}^{P2}$ implies the j^{th} dimension, F_i^{P2} denotes its corresponding objective function and lastly, I represents the random number between $\{1,2\}$ respectively. Figure 9 showcases the flowchart of the FFA-ANN MPPT controller.

III. RESULTS AND DISCUSSION

This section analyzes an outcomes of developed power quality enhancement utilizing SAPF with adaptive inductor step-up converter in MATLAB/Simulink software. Table 2 reveals the parameters of developed research.

Table 2: Parameter Specification.

Parameter	Specification
AC Source	
Load Inductance	10mH
Load Resistance	100Ω
PV system	
Total Power	10000 W
Panel's peak power	250 W
Voltage (Open circuit)	37.25V
Current (Short circuit)	8.95 A
Maximum Peak Voltage	29.95 V
No of cells in series connection, N_s	10
No of cells in shunt connection, N_p	4
AISC converter	
L_x	45mH
L_y	700 mH
C_1, C_2, C_3, C_4, C_5	22 μF
C_0	2200 μF
Switching Frequency	10 kHz

Source: Authors, (2026).

Case 1: With step magnitude +0.2

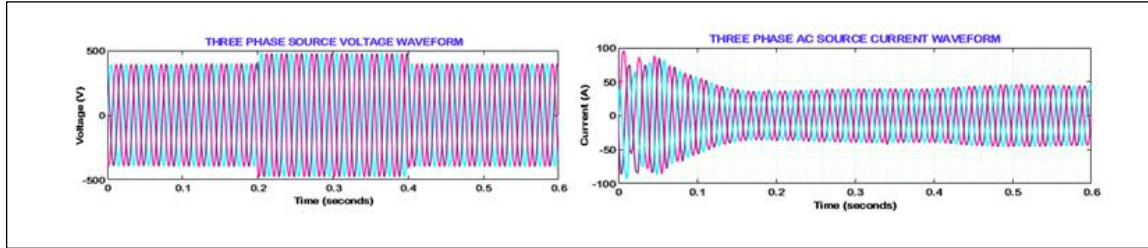


Figure 10: Waveform of 3 ϕ AC source.

Source: Authors, (2026).

Figure 10 represents the waveform of 3 ϕ AC source current and under voltage sag condition. In the beginning, the source voltage is maintained a stable value of 420 V and after 0.2 s, it is increased to 480 V. It is concluded that the source voltage is impacted by PQ issue of voltage sag of 60 V from 0.2 to 0.4s. Meanwhile, the source current is randomly varied and is settled at 40 A without variations.

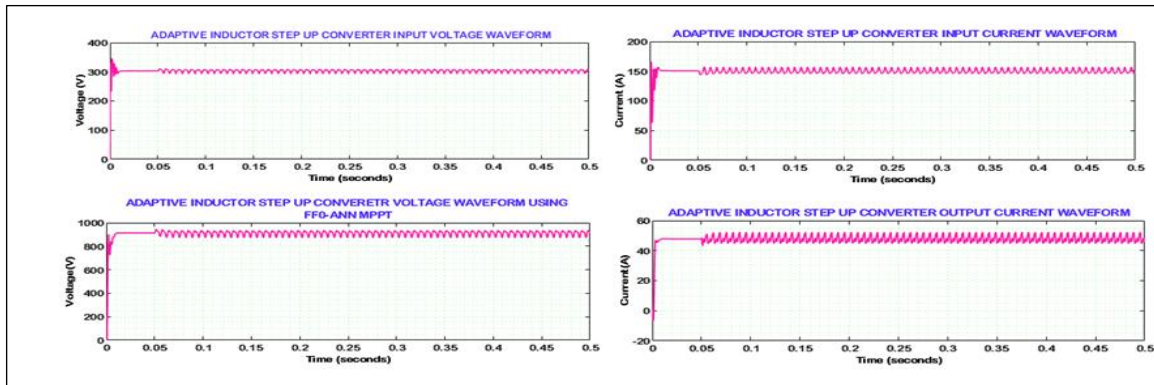


Figure 11: Behaviour of AISC.

Source: Authors, (2026).

The behaviour of AISC is depicted in Figure 11, in which the input voltage has initial variations and then, it sustained at 300 V with little oscillations. Also, an input current is gradually increased and settled at 150 A with small distortions. There by, an output voltage is increased slowly and maintained at 900 V with little changes and an output current is gradually raised and sustained at 46 A in the entire system.

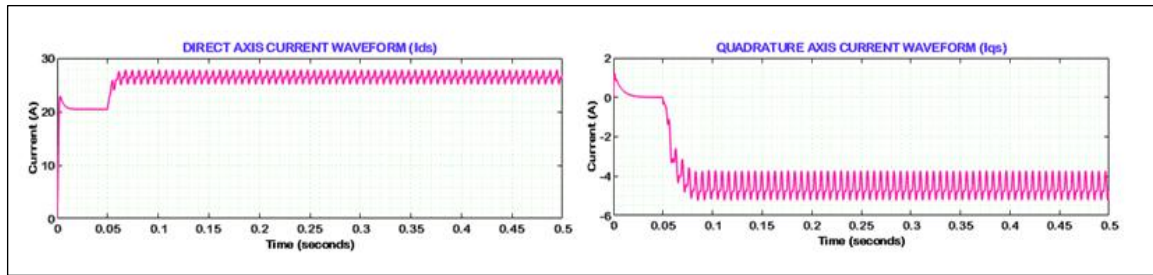


Figure 12: Waveform of direct and Quadrature Axis Current.
Source: Authors, (2026).

Figure 12 presents the waveform of direct and quadrature axis current, in which the current of direct axis is randomly changed in the beginning and stabilized at 26 A with more distortions. Subsequently, the current of quadrature axis is slowly reduced and is settled at 4 A with more distortions throughout the system. It is implemented via a vector control (field-oriented control) approach, which is standard in modern grid-tied inverter systems to meet grid code necessities for both active and reactive power control.

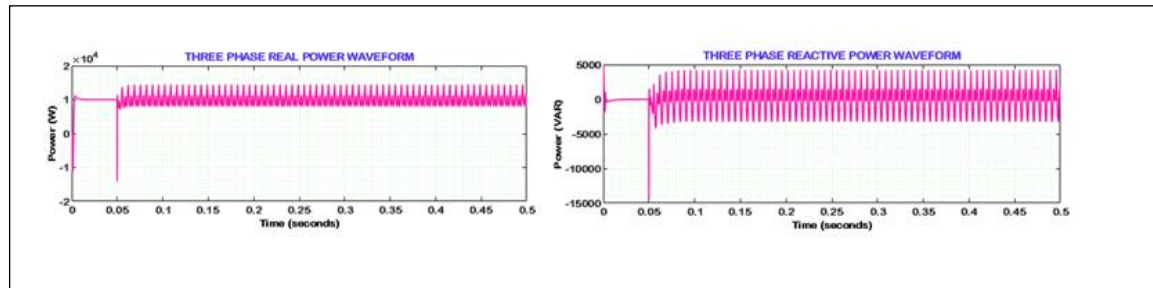


Figure 13: Waveform of Power.
Source: Authors, (2026).

The waveform of real and reactive power is depicted in Figure 13. The real power is maintained at $1.5 \times 10^4 W$ with little distortions and reactive power has random changes in the beginning and is stabilized at 4000 VAR with random variations in the entire system, thereby improving power quality.

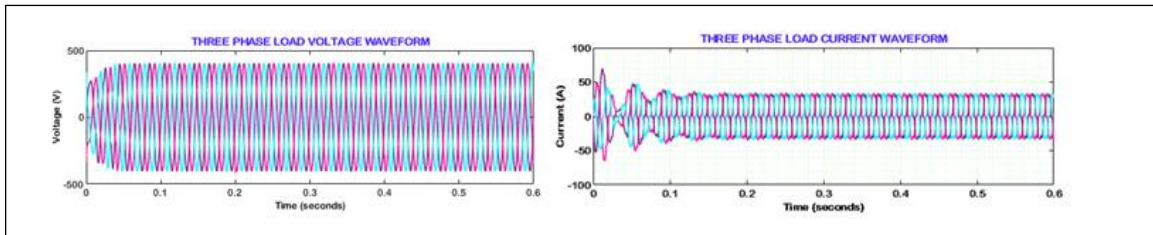


Figure 14: Waveform of Load
Source: Authors, (2026).

Figure 14 displays the waveform of load current and voltage. The current on load side is slowly raised and is maintained at 420 A throughout the system. Likewise, the load voltage has oscillations in the starting period and is stabilized at 30 A in the entire system.

Case 2: With step magnitude -0.2

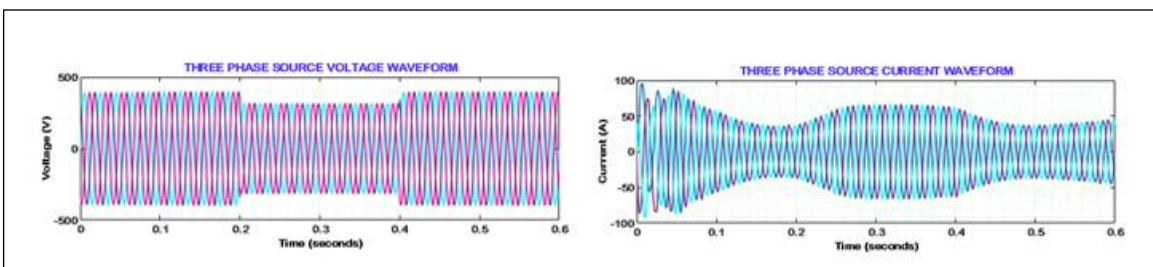


Figure 15: Waveform of 3 ϕ source.
Source: Authors, (2026).

The waveform of 3ϕ source current and voltage is revealed in Figure 15. The source voltage is initially sustained at 480 V and after 0.2s, it is reduced to 420 V (voltage swell of 60 V) and remained at 480 V. Meanwhile, the source current is varied in the beginning and settled at 40 A.

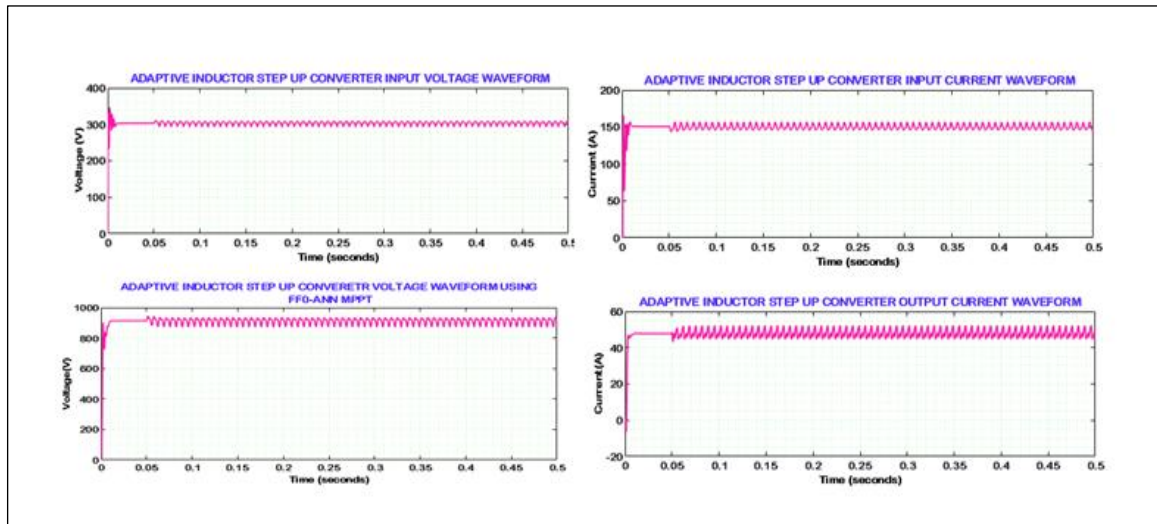


Figure 16: Behaviour of AISC.
Source: Authors, (2026).

Figure 16 depicts the behaviour of AISC and an input voltage is maintained at 300 V with little oscillations. Subsequently, an input current is varied in the beginning and maintained at 150 A with small variations. Likewise, an output voltage is slowly raised and is sustained at 900 V with little fluctuations because of the exploitation of FFO based ANN-MPPT controller. Consequently, an output current is gradually increased and settled at 45 A with more distortions.

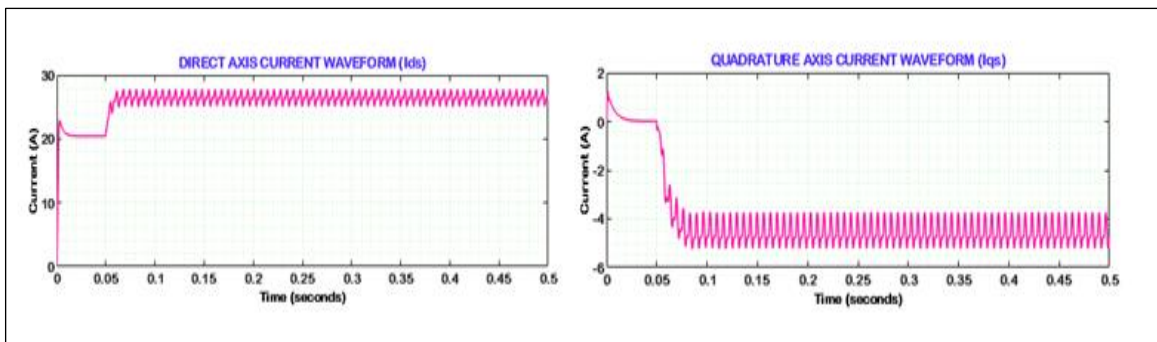


Figure 17: Waveform of Direct and Quadrature Axis Current.
Source: Authors, (2026).

The waveform of direct and quadrature axis current is represented in Figure 17. The current of direct axis is slowly improved and is sustained at 28 A and current of quadrature axis is gradually reduced in the starting period and is maintained at -4 A with oscillations.

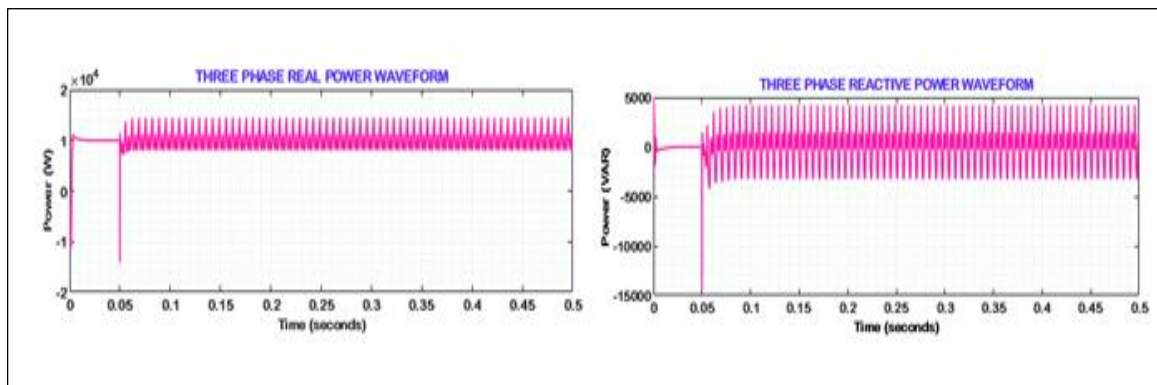


Figure 18: Waveform of Power.
Source: Authors, (2026).

Figure 18 indicates the waveform of real and reactive power. The real power is maintained at $1.5 \times 10^4 W$ meanwhile, the reactive power is sustained at 4000 VAR with random distortions, ensure effective and consistent power delivery.

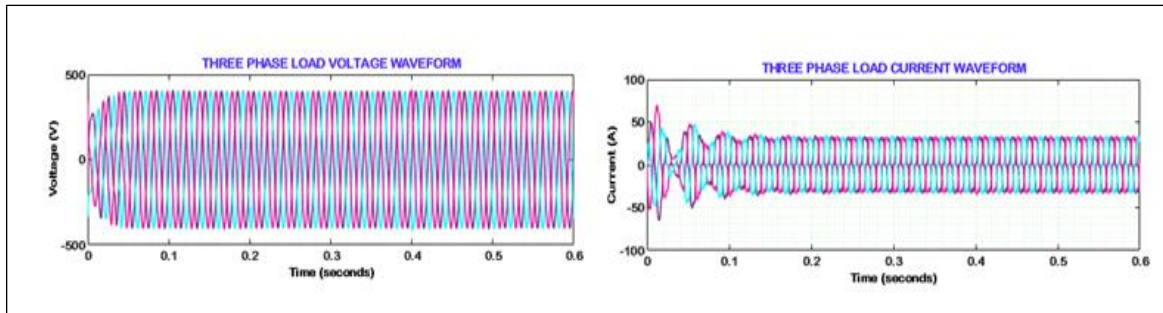


Figure 19 Waveform of Load Current and Voltage.

Source: Authors, (2026).

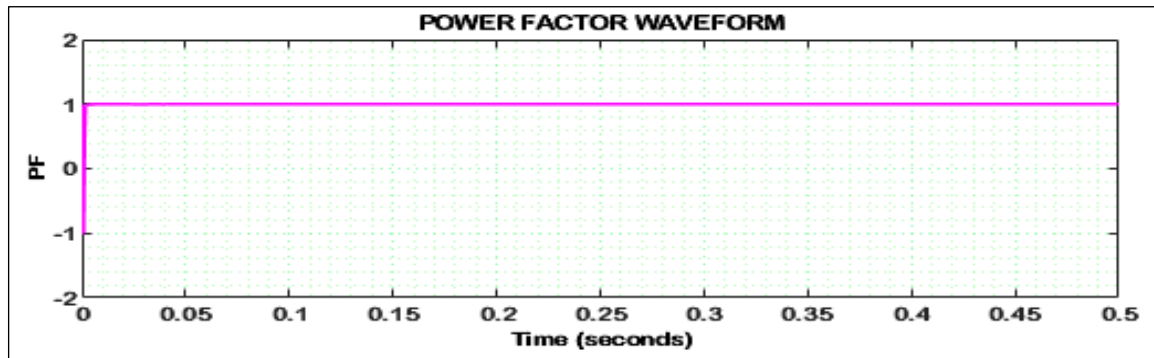


Figure 20: Waveform of Power Factor.

Source: Authors, (2026).

The waveform of load current and voltage is seen in Figure 19. The voltage on load side has variation in an initial period and sustained at 420 V while the load current is arbitrarily varied and sustained at 30 A in the entire system. Figure 20 represents the waveform of power factor and is maintained at unity value throughout the system.

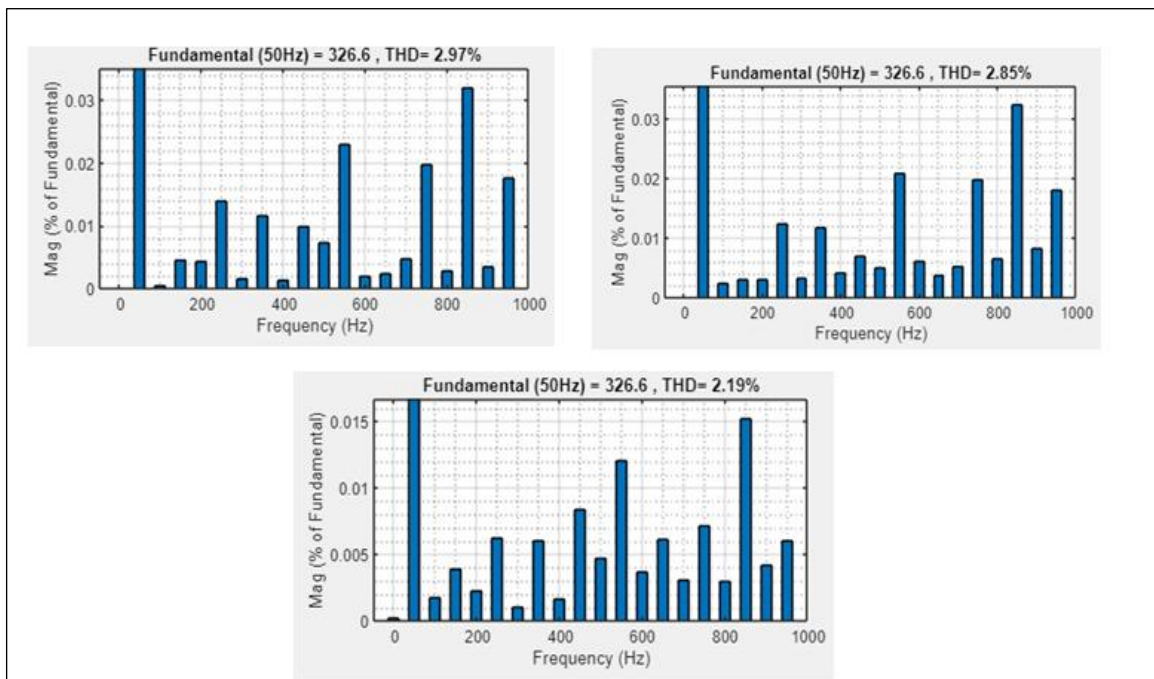


Figure 21: THD of Reduced Switch 17 Level MLI.

Source: Authors, (2026).

Figure 21 depicts the THD of reduced switch 17 level MLI for R, Y and B phases. In the R Phase, the THD is 2.97%, representing a moderate presence of harmonics primarily at integer multiples of the fundamental frequency. The Y phase has an improved performance with a THD of 2.85%, indicating the efficiency of optimized switching methods or modulation approaches in lessening the harmonic content.

The B phase has the lowest THD of 2.19%, reflecting superior harmonic suppression. This significant reduction confirms the capability of the reduced switch 17-level MLI to generate high-quality output voltage with minimal harmonic pollution. The reduced switch count not only shortens the circuit design and diminishes switching losses but also efficiently alleviates harmonics, ensuing better voltage waveform and compliance with grid power quality standards.

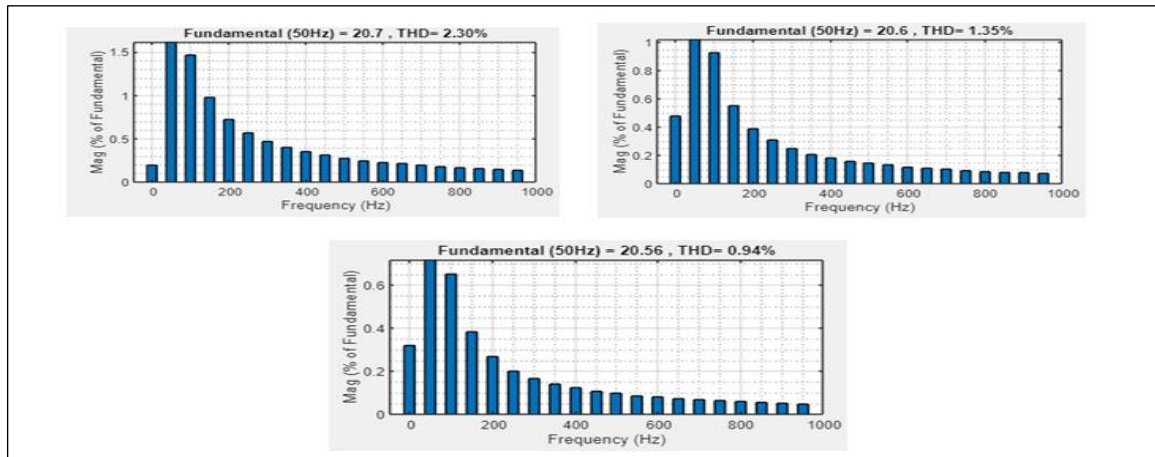


Figure 22: THD of Grid.
Source: Authors, (2026).

The THD of grid for R, Y and B phases is depicted in Figure 22. The R phase has the THD of 2.30%, designates moderate distortion in the grid waveform. Then, the Y phase has a better harmonic profile with a reduced THD of 1.35%, signifying enhanced power quality due to better filtering or control schemes applied to the grid-connected system. The B phase demonstrates the most optimal condition with a minimal THD of 0.94%, endorsing effective mitigation of distortion and near sinusoidal voltage output at the grid interface. It exhibits outstanding harmonic suppression, vital for sustaining voltage quality and complying with international grid standards.

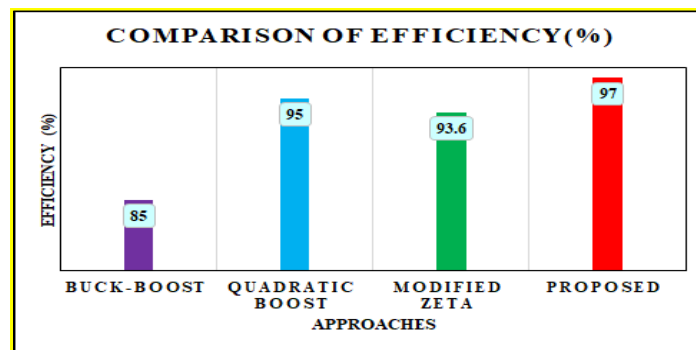


Figure 23: Comparison of Converter Efficiency.
Source: Authors, (2026).

Figure 23 represents the comparison of efficiency for Buck-Boost [27], Quadratic Boost [28], Modified Zeta [29] and developed converter. The highest efficiency of 97 % is attained by the developed converter than Buck-Boost(85 %), Quadratic Boost (95 %), Modified Zeta converters (93.6 %). It highlights that the developed converter attains comparable peak performance to the Quadratic Boost but potentially with operational advantages, thereby emphasizing the better performance of the developed converter over the other converters.

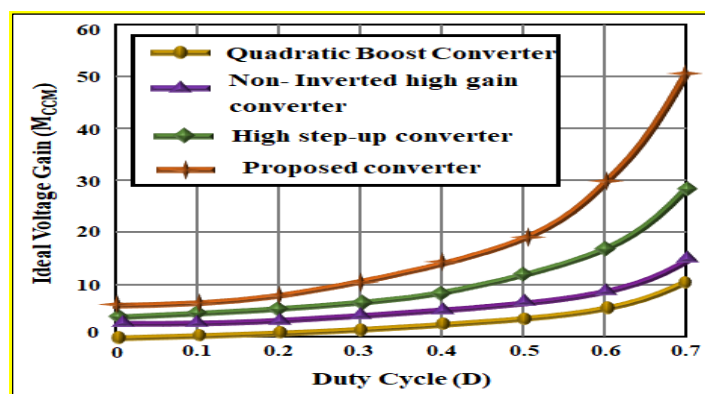


Figure 24: Analysis of Voltage Gain.
Source: Authors, (2026).

The analysis of voltage gain for developed approach with Quadratic boost [30], Non-inverted high gain [31], high stepup [32] converter is presented in Figure 24. The developed converter consistently exhibits the highest voltage gain across all duty cycle values, with a particularly sharp increase beyond a duty cycle of 0.4. The High Step-Up converter follows, showing moderate improvement, especially after 0.5 duty cycle. The Non-Inverted High Gain Converter and Quadratic Boost Converter exhibit comparatively lower voltage gains in the entire range. It validates the greater boosting ability of the developed converter, making it highly appropriate for applications requiring maximum voltage gains at moderate to high duty cycles.

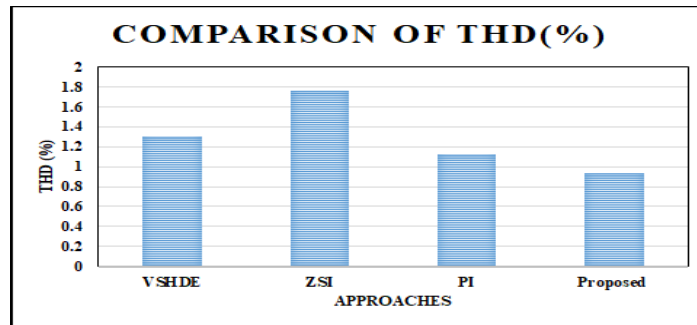


Figure 25: Comparison of THD (%).

Source: Authors, (2026).

The THD is compared for developed and Variable Scaling Hybrid Differential Evolution (VSHDE) [33], Z-source inverter (ZSI) [34], Proportional Integral (PI) [35] approach is depicted in Figure 25. The developed approach has the better THD of 0.94 % than VSHDE(1.30%), ZSI (1.76%) and PI (1.13%) approaches, indicating the overall power quality of system is enhanced. The ZSI method records the lowest THD at 1.13%, indicating superior harmonic performance. The VSHDE controller follows with a THD of 1.3%. The PI controller has the highest THD at 1.76%, signifying relatively poorer harmonic suppression. It emphasizes the effectiveness of developed approach in minimizing harmonic distortions compared to other methods.

Table 3: Analysis of Source current THD (%).

Approaches /Phases	R	Y	B
GRU	3.35	3.34	3.20
Proposed	2.97	2.85	2.19

Source: Authors, (2026).

The analysis of source current THD for R, Y and B phase is represented in Table 2. The developed approach has the lowest THD of 2.97%, 2.85% and 2.19 % than the Gated Recurrent Unit (GRU) [36] approach, indicating the overall power quality is enhanced with the aid of developed approach.

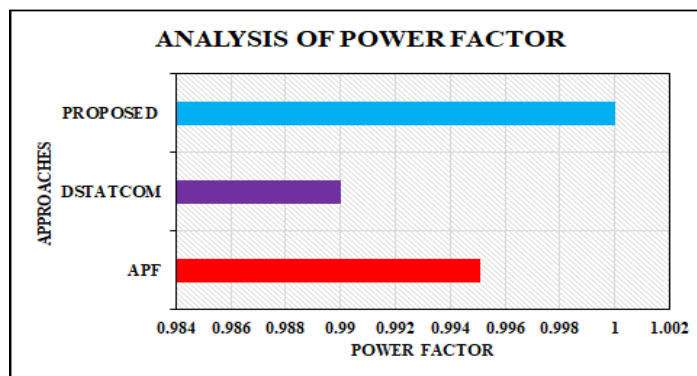


Figure 26: Analysis of Power Factor.

Source: Authors, (2026).

Figure 26 represents an analysis of power factor for developed approach with Distribution Static Compensator (DSTATCOM) [37] and APF [38]. The developed approach attains the maximum power factor of 1 that denotes better reactive power compensation and improved system efficacy. In contrast, the APF has power factor of 0.9951 whereas the DSTATCOM has the value of 0.99. The improved performance of the proposed method highlights its ability in better mitigating power quality issues and assuring enhanced voltage regulation and load balancing in distribution systems.

IV. CONCLUSION

The proposed system designed and developed using the SAPF based PQ enhancement approach effectively enables improves PQ in power distribution systems while providing enhanced reactive power compensation. In addition to this, the integration of RES based PV system assures consistent and sustainable power supply, and the deployment of AISC further ensures enhanced regulation of PV power production with increased voltage gain and reduced losses.

The employment of FFO based ANN-MPPT offers maximum power extraction from PV along with continuous, accurate and effective tracking of MPP with increased convergence speed. Moreover, the utilization reduced switch 17 level MLI enables to attain higher level output voltages with enhanced conversion of output voltage before proceeding it to the grid making it applicable for grid application. Therefore, to validate the proposed system MATLAB/Simulink is utilized and the obtained results assures that, proposed system shows effective improvement of PQ while reducing losses and enhanced management of voltage stability and reliability at PCC. Thus, the overall system enables improved system stability, reliability and efficiency with enhanced quality of output power providing positive impacts on power distribution systems.

V. AUTHOR'S CONTRIBUTION

Conceptualization: Gadupudi Lakshminarayana, Krishna Prakash Arunachalam, Pranita Chavan, M Pandikumar.

Methodology: Krishna Prakash Arunachalam, Pranita Chavan, M Pandikumar.

Investigation: Gadupudi Lakshminarayana, Krishna Prakash Arunachalam.

Discussion of results: Gadupudi Lakshminarayana, Krishna Prakash Arunachalam, Pranita Chavan, M Pandikumar.

Writing – Original Draft: Gadupudi Lakshminarayana.

Writing – Review and Editing: Krishna Prakash Arunachalam, Pranita Chavan, M Pandikumar.

Resources: Krishna Prakash Arunachalam, Pranita Chavan, M Pandikumar.

Supervision: Krishna Prakash Arunachalam, Pranita Chavan, M Pandikumar.

Approval of the final text: Gadupudi Lakshminarayana.

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