



ANALYSIS OF THD, RMS OUTPUT VOLTAGE AND VOLTAGE STREE ACROSS SWITCHING DEVICE FOR 1500V DC BUS THREE LEVEL ANPC INVERTER

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ABSTRACT

Multilevel topologies have been used more frequently for high voltage applications in order to produce a staircase voltage waveform with total harmonic distortion (THD). This has increased interest in high-power systems and prompted the continuous development of advanced topologies. This paper discusses the advantages of the active neutral point clamp (ANPC) topology over neutral point clamp (NPC), flying capacitor neutral point clamp (FCNPC) and T-type neutral point clamp (TNPC) topologies for a 1500V direct current (DC) bus, focusing on superior loss distribution, elimination of passive clamping components, and the ability to utilize lower-voltage-rated switches. To investigate the THD for three-level ANPC inverter, a number of pulse width modulation (PWM) approaches based on carrier wave and reference-wave modification are applied. Phase opposition pulse width modulation (PODPWM), phase disposition pulse width modulation (PDPWM), and alternative PODPWM (APODPWM) and phase-shifted PWM (PSPWM), triangle saturated clamp mode PWM (TSCMPWM) are evaluated based on the carrier signals phase arrangement. The bus clamping PWM (BCPWM), trapezoidal triangle PWM (TRPWM), third harmonic injected PWM (THIPWM), three-phase sinusoidal signals with a 13th harmonic signal PWM (THISDPWM) are addressed based on the modification by inserting an additional signal into the sinusoidal wave to obtain the new reference wave. Also, the parasitic inductance model of ANPC topology is simulated. To use a 1200 V switching device, the most efficient PWM technique for a 1500 V DC bus three-phase three-level ANPC inverter is determined by comparing the root mean square (RMS) value of phase voltage, THD and peak voltage across the switching device. PSIM software has been used to simulate a three-level inverter using various PWM techniques.



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I. INTRODUCTION

India's per capita electricity consumption grew from 957 kWh in 2013–14 to 1,395 kWh in 2023–24, a 45.8% increase (438 kWh) thanks to 129 GW of renewable energy capacity. The solar energy capacity of India reaches 94.17GW in 2024 [1] [2]. As of November 2024, the nations installed and pipeline solar projects totaled 261.15 GW, indicating a robust pipeline for future development and expansion in the solar industry. Conventional two-level inverters have been found to be unsuitable because they have fewer output voltage levels and, consequently, higher harmonics in the injected grid current. The multi level inverters (MLI) have always provided higher-quality output voltage waveforms with lower harmonics and THD, reduced switch dv/dt stress, and required fewer passive filters. By decreasing the current and increasing the voltage to 1000V or 1500V DC from the array, the power levels can be kept constant. Because of the decrease in current, the design requires less copper and smaller power conducting components. The stress on electrical components is also decreased by the decrease in di/dt [3] [4].

Three-level NPC inverter load power factor determine the different communication loop for switching that causes the different losses among the semiconductor devices. These two loops' different physical path lengths result in different stray inductance values. Consequently, the semiconductor devices dissipate uneven quantities of power loss and undergo varying amount of electrical stress [5]. TNPC has greater power conversion efficiency particularly at lower switching frequencies. However, because this design necessitates higher blocking voltage rated semiconductor chips, it is less economically appealing for high voltage applications. Additionally, because of the uneven voltage stress on the semiconductor devices, the T-type topology has an uneven loss distribution among the semiconductor devices. FCNPC inverter's overall power density is reduced by the flying capacitor's physical size. In power electronic system, capacitor is the component with shortest lifetime, which could lower the mean time between the failures for the entire system. Even maintaining the precise voltage across these flying capacitors requires complex control algorithms. Under unbalanced conditions, the capacitor voltage can deviate, leading to a distorted output waveform that increases device stress [6]. The major drawback of other topologies is uneven semiconductor loss distribution can be addressed by the ANPC topology. Its design gives the neutral point current two adaptable, redundant pathways. Regardless of the power factor of the connected load, the management system can actively manage and balance power losses across all switching devices due to this built in redundancy. Additionally, the ANPC topology permits the use of semiconductor devices with lower voltage ratings in high voltage applications. Active loss balancing and the use of less expensive, lower rated switches makes the ANPC inverter very desirable for high-power system [7]. In this paper three-level ANPC inverter for a 1500V DC bus is examined. The three goals are to optimize the RMS voltage, decrease the output voltage THD, and find the PWM techniques that minimize the voltage stress across the switching device below 1200V limit. Through detailed simulation in PSIM software this paper provides multiple carrier and reference-based modulation techniques to determine the most suitable approach for high voltage applications. This work is intended to perform the simulation using the trapezoidal carrier signal in different positions and compare it with seven different reference signals generated to optimize the THD and RMS output voltage using different switching patterns.

II. THEORETICAL REFERENCE

This paper's literature evaluation was conducted using power topology and control strategy adapted to generate a 3-level output voltage. MLI topologies are classified by various ways like the convectional and non-convectional [7], based on single DC source and multiple DC source [8], based on voltage source inverter and current source inverter, based on H-bridge and non H-bridge topologies [9] [10], based on symmetric DC source and asymmetric DC source [11] [12]. A single DC source is used in a combination of centralized, medium voltage grid-connected inverters with different power ratings. This is commonly referred to as the central inverter system. In central inverter with single DC source the topologies like NPC, ANPC, FCNPC and TNPC are used. The comparison of these topologies is given in Table 1.

Table 1: Comparison of three level topologies based on component.

Component	NPC	ANPC	FC NPC	TNPC
Freewheeling diodes	6	0	0	0
Switching devices	12	18	12	18
DC link capacitor	2	2	2	2
Flying capacitor	0	0	2	0
Balancing Capacitor	0	0	1	0
DC Sources	1	1	1	1
Total Components used	21	21	18	21

Source: Authors, (2026).

Improving multilevel capabilities for high voltage situations is the focus of recent research. When compare to other three level structures, ANPC arrangement shows significant advantages, particularly in terms of control and electromagnetic interference suppression. In order to improve waveform quality and operating efficiency, modern research investigates sophisticated modulation techniques that go beyond tradition sinusoidal pulse width modulation, such as harmonic augmentation and switching sequence modification. Nevertheless, there isn't a thorough analysis in literature that incorporates several advanced modulation techniques into 1500 V DC bus ANPC inverter while also assessing semiconductor stress factors and outlining workable control strategy. This work fills that gap by methodically evaluating several carrier and reference signal combinations at high voltage and developing and open implementation approach [13-15]. The mentioned PWM pulses are produced using the Sin-trapezoidal triangle comparison techniques [16]. Unlike other optimized PWM techniques, these methods do not require search databases for the desired transitioning states of power switches, deep offline computations, or optimization techniques. This technique is beneficial due to its low switching losses, decreased output voltage waveform harmonics, and ease of implementation. For this reason, multi-level inverter (MLI) switch triggering pulses can be produced effectively using these techniques for comparison. In this method the reference signal (V_{sin}) is compared with the trapezoidal triangle carrier signal (V_{carr}) to generate the PWM pulses [17] [18]. Limiting the magnitude of a triangular wave produces that trapezoidal wave. Figure1 displays the gate pulse that is produced when a Sin wave is compared to the trapezoidal reference signal. Based on the phase arrangement these techniques further classified as given below [19-26]:

II.1 PHASE ARRANGMENT TECHNIQUES

II.1.1 Phase Disposition PWM (PDPWM):

This technique includes vertically shifting two carrier signals with DC offset equal to the carrier magnitude (V_{carr1_PD} and V_{carr2_PD}) on either side of the zero reference (V_{sin}) for a three-level inverter.

The same carrier signals in terms of frequency, amplitude, and phase are used in this, as shown in Figure 1(a). As illustrated in Figure 1(a), the PWM pulse for a three-level inverter is generated by separately comparing the carrier signals with a reference signal.

II.1.2 Phase Opposition Disposition PWM (PODPWM):

With the PODPWM technique, each carrier signal (V_{carr1_POD} and V_{carr2_POD}) has a distinct phase but the same frequency and amplitude. Two 3-level inverter carrier signals above the zero-reference frame are 180° out of phase with the carrier signals below the zero reference, as shown in Figure 1(b).

II.1.3 Alternative Phase Opposition Disposition PWM (APODPWM):

As seen in Figure 1(c) the switching signal for a three-level inverter is produced by placing two identical carrier signals (V_{carr1_APOD} and V_{carr2_APOD}) alternately in phase opposition and comparing them to a sinusoidal reference (V_{sin}).

II.1.4 Phase Shifted PWM (PSPWM):

For 3-level inverter, there are 2 carrier signals with equal frequency and magnitude that undergo equal phase shifts during a single switching period. Two carrier signals (V_{carr1_PS} and V_{carr2_PS}) for a three-level inverter, as illustrated in Figure 1(d), have a 90° horizontal phase shift but the same frequency, amplitude, and DC offset. The proper PWM pulses are then produced by comparing the carrier signals and the sinusoidal reference (V_{sin}), as shown in Figure 1(d).

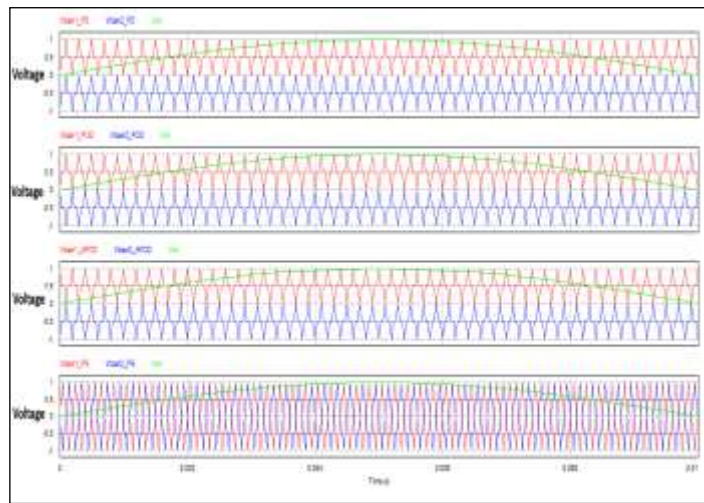


Figure 1: Different Trapezoidal Triangle Carrier based PWM method for ANPC inverter (a) PDPWM (b) PODPWM (c) APODPWM (d) PSPWM.

Source: Authors, (2026).

III. MATERIALS AND METHODS

In NPC inverter topology when it's operated on 1500V DC bus with half a rating of the device can have very high dv/dt at the switching and that may damage the switching device. In T-NPC topology the switching device can block the entire DC bus voltage and hence the voltage rating of the switching device depends upon the DC bus voltage so when operates on 1500V DC bus system the switching device rating should be very high and hence the cost of the overall system will increase FC-NPC topology has major advantages over NPC, ANPC and TNPC topology in term of capacitor voltage balancing but the major disadvantage of this topology is the larger number of capacitor and complex control mechanism. The ANPC topology first proposed by ABB. Figure 2 depicts the structure of a three-level ANPC inverter that uses switching devices in place of the clamp diodes in a three-level NPC topology [27]. The switching states of the 3L-ANPC topology are summarized in Table 2; it includes four extra zero states in addition to the same positive and negative switching states as the 3L-NPC converter.

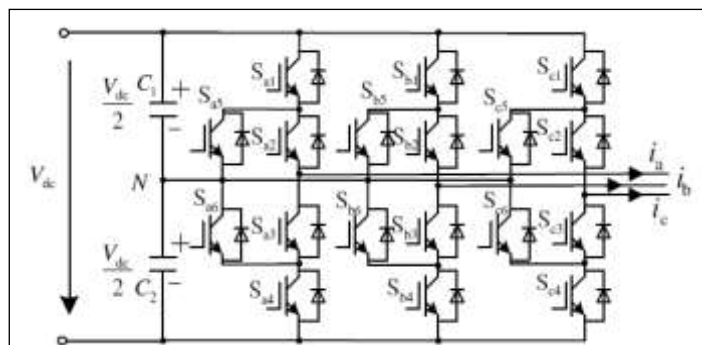


Figure 2: Topology for Three level ANPC inverter.

Source: Authors, (2026).

Table 2: Switching states for ANPC topology.

State	T1	T2	T3	T4
P	1	1	0	0
0	0	1	0	0
0	0	1	0	1
0	1	0	1	0
0	0	0	1	0
N	0	0	1	1

Source: Authors, (2026).

III.1 GENERATION OF DIFFERENT REFERENCE WAVE FOR THREE-LEVEL ANPC INVERTER

III.1.1 Sinusoidal Pulse Width Modulation (SPWM):

Equation 1 describes the fundamental equation for three phase system. V_r represents the reference signal with respect to the phase Y which is phase sifted by 120° . ma defined the modulation index and f is fundamental frequency of the system as shown in Figure 2(a) [28-30]. For each phase lag that has to be compare with carrier signal to generate the PWM pulses. The inherent cancellation of carrier harmonic multiples in line-to-line voltage is the advantage of using this method.

$$V_r = ma \sin\left(2\pi ft - \frac{2\pi(Y-1)}{3}\right), Y \in \{1,2,3\} \quad (1)$$

III.1.2 Third harmonic Injected PWM (THIPWM):

Equation 2 describes the third harmonic injected PWM method which is intensification of SPWM techniques. A third harmonic component is added on top of the fundamental component to create the third harmonic injected PWM. As illustrated in Figure 2(b), adding a third harmonic component to the output and reference signals increases the fundamental's maximum amplitude. Since the addition cancels out in the voltage difference between phase as a zero-sequence component, it doesn't show off in the final line to line output voltage. Through the removal of the third harmonic component, this technique enhances the DC supply's utilization [31].

$$X = K * \sin(3 * \omega * t); K = 0.19$$

$$V_r = ma \sin\left(2\pi ft - \frac{2\pi(Y-1)}{3}\right) + X, Y \in \{1,2,3\} \quad (2)$$

III.1.3 Ninth Order Harmonic Injected PWM:

The ninth order harmonic injected PWM method is slight variation in previously discuss method. As ninth order harmonics is added to the THIPWM method to generate the reference waveform V_r as shown in Figure 2(c). By injecting the ninth order component its further flatter the combined reference wave peak. Therefore, the method describe in Equation 3 is essential for maximizing the DC bus consumption and improving the quality of inverter output voltage by reducing the harmonic voltage content at higher modulation index [32].

$$P = K * \sin(3 * \omega * t); K = 0.19$$

$$Q = M * \sin(9 * \omega * t); K = 0.029$$

$$V_r = ma \sin\left(2\pi ft - \frac{2\pi(Y-1)}{3}\right) + P + Q, Y \in \{1,2,3\} \quad (3)$$

III.1.4 Thirteenth Orders Harmonic Injected PWM:

In this method the thirteenth order reference wave is created by adding 13th order into the saturated fundamental component which magnitude is limited between -1.5 to 1.5 and the resultant waveform will be added to the fundamental Sin wave and hence the peak amplitude is modified as shown in Figure 2(d). By adding the 13th order harmonic component outline in Equation 4 operates on effective higher modulation index, bringing the DC bus usage close to the maximum of 1.1547 and bringing the harmonic content down [32].

$$P = q * B_m * \sin(\omega * t + \alpha); q \in [-1,1], B_m \in [-1.5,1.5], \alpha = 0^\circ, -120^\circ \text{ and } -240^\circ$$

$$Q = r * A_m * \sin(13 * \omega * t + \alpha); r = 0.01$$

$$V_r = ma \sin\left(2\pi ft - \frac{2\pi(Y-1)}{3}\right) + P + Q, Y \in \{1,2,3\} \quad (4)$$

III.1.5 Sixty Degree Bus Clamp Pulse Width Modulation (SDBCPWM):

A variation on the third harmonic injected PWM technique, the sixty degree PWM method involves holding the switch high (or low) for sixty degrees of each half cycle of the fundamental.

As a result, switching losses are decreased and the fundamental voltage component is raised. The periodic signal obtained by adding all of the harmonics with the fundamental is depicted in the Figure 2(e). Two of the inverter leg switch at higher carrier frequency and one leg clamped at DC bus for one sixth of fundamental cycle and hence for clamped leg the switching loss is eliminated. Equation-5 is the optimization method that increases efficiency, which make it the appropriate for higher power application [33].

$$V_r = \sin(\omega * t + \alpha) + f_1(\theta)\{V_c - \max(V_r, V_y, V_b)\} + f_2(\theta)\{-V_c - \min(V_r, V_y, V_b)\} \quad (5)$$

$$\alpha = 0^\circ, -120^\circ \text{ and } -240^\circ$$

$$f_1(\theta) = 0 \text{ (when } 0^\circ < \theta < 60^\circ \text{)}$$

$$f_1(\theta) = 1 \text{ (when } 60^\circ < \theta < 120^\circ \text{)}$$

$$f_2(\theta) = 1 \text{ (when } 0^\circ < \theta < 60^\circ \text{)}$$

$$f_2(\theta) = 0 \text{ (when } 60^\circ < \theta < 120^\circ \text{)}$$

III.1.6 Thirty Degree Bus Clamp Pulse Width Modulation (TDBCPWM):

The clamping operation in Equation 6 restrict the modulating signals at thirty degree of every half cycle in both positive and negative cycle as shown in Figure3 (f). As compare to SDBCPWM technique, this method gives more balance operation. Conversely, the harmonic distortion introduced in the output current is also reduced because the deviation from the ideal sinusoidal reference is shorter in duration. This results in a more favourable trade-off between efficiency and waveform quality for many applications. Therefore, Equation 6 represents an optimized modulation technique suitable for systems where both switching loss reduction and acceptable current ripple are important design considerations [33].

$$V_r = \sin(\omega * t + \alpha) + f - (\theta)\{V_c - \max(V_r, V_y, V_b)\} + f_1 - \theta\{-V_c - \min(V_r, V_y, V_b)\} \quad (6)$$

$$\alpha = 0^\circ, -120^\circ \text{ and } -240^\circ$$

III.1.7 Triangle Saturated Common Mode Pulse Width Modulation (TSCMPWM)

Equation 7 describes that the sinusoidal reference wave is added by a saturated triangle wave to generate the TSCMPWM signal as shown in Figure3 (g). This term is produced by saturating (or limiting) a regular sinusoidal or third-harmonic injection common-mode signal against a virtual envelope that is derived from the amplitude of the triangular carrier waveform; it is not a fixed harmonic [34] [35].

$$X = 2 * \pi * C * \sin -1 \{\sin(3 * \omega * t)\}$$

$$Y = V_1$$

$$Y = 0.11C \text{ (when } X > 0.11C \text{)}$$

$$Y = -0.11C \text{ (when } X < -0.11C \text{)}$$

$$V_r = \sin(\omega * t) + Y, V_y = -\sin\left(\omega * t - \frac{2\pi}{3}\right) + Y, V_b = \sin\left(\omega * t + \frac{2\pi}{3}\right) + Y \quad (7)$$

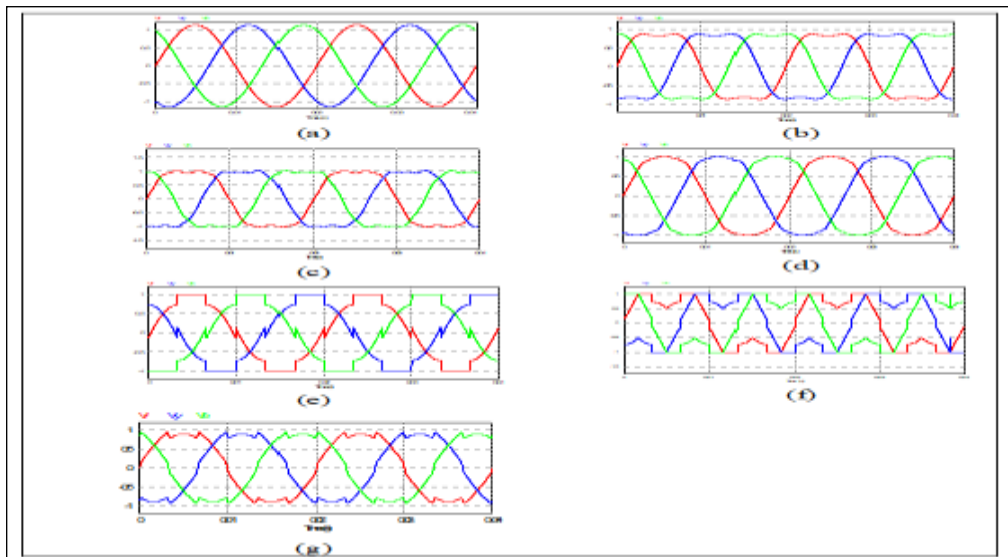


Figure 3: The modulating signal with different PWM techniques.

Source: Authors, (2026).

IV. SIMULATION MODEL OF THREE-LEVEL ANPC INVERTER

In this paper simulation is carried out with following parameters. The simulation parameters are selected as below:

$V_{dc}=1500V$ this is a standard voltage for modern utility-scale PV systems, $C_1= 28.2mF$, $C_2= 28.2mF$, The capacitance value was chosen to limit the DC-link voltage ripple to below 2%, as per common design practice for stable inverter operation [28] $R_{load}= 27m\Omega$, $L_{load} = 2400\mu H$, These values represent a typical low-impedance, high-power load, drawing current in the range of hundreds of amperes, consistent with multi-megawatt inverter ratings. $L_q = 30nH$, $L_{qclamp} = 120nH$, $L_{qinv} = 120nH$, $L_{bus} = 120nH$. These values, based on the work of [29], are critical for accurately modelling voltage spikes during switching transients and are representative of practical busbar and package parasitic. The modulation index is taken 1 for comparison of each methods.

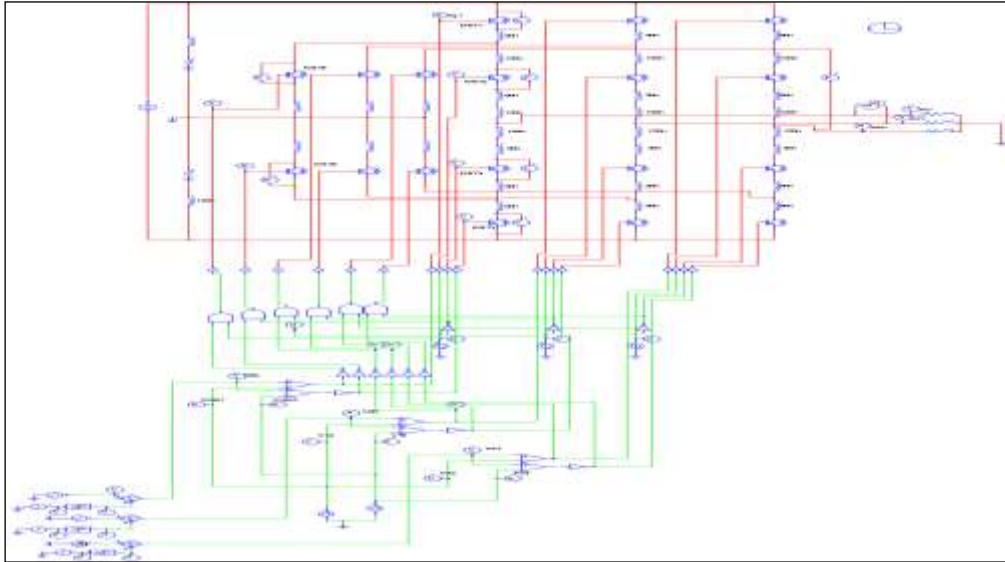


Figure 4: Simulation schematic diagram of generating PWM1 fed TSCMPWM.

Source: Authors, (2026).

A typical value for high-power insulated gate bipolar transistor (IGBT) based inverters, balancing switching losses and harmonic performance. 1200V IGBTs were selected over Silicon carbide (SiC) for this specific analysis due to their cost-effectiveness and proven reliability in multi-megawatt industrial drives and renewable energy inverters. While SiC offers lower switching losses, the maturity, ruggedness, and lower cost of 1200V IGBTs make them a prevalent choice in current 1500V DC system designs. [20] To generate the PWM pulses carrier wave can be obtained by using trapezoidal wave with different combination of PDPWM, PODPWM, APODPWM and PSPWM techniques and its compare with the reference wave generated by different techniques. Figure 4 shows the ANPC inverter with TSCMPWM reference signals in PWM1 type signal generation. Figure 5 (a) to (d) illustrates the PWM1, PWM2, PWM3, and PWM4 logics used to generate the gate pulses for the R-phase switches S1 through S6.

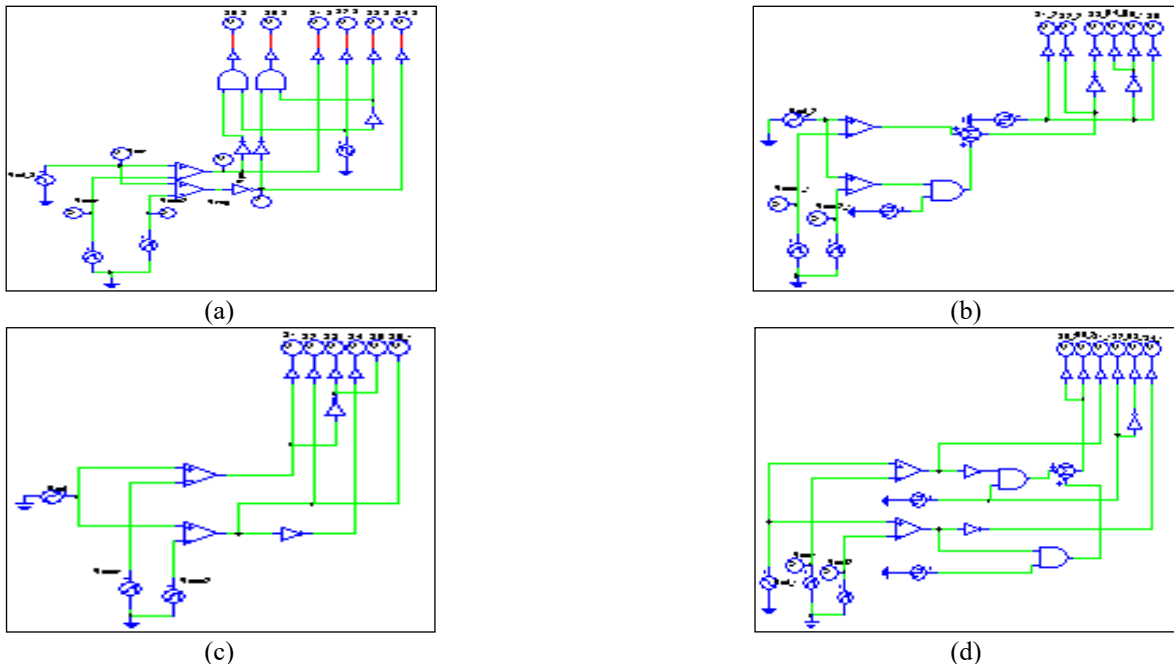


Figure 5: Generation of PWM for switch S1 to S6 for SPWM techniques (a) PWM1 (b) PWM2 (c) PWM 3 (d) PWM4.

Source: Authors, (2026).

V. SIMULATION RESULTS

PSIM software is used for the simulation and the data presented here in different sections. The modulation of output phase voltage and the peak voltage across each switching devices. To generate the gate pulses of PWM1, PWM2, PWM3 and PWM4 techniques for switch S1 to S6 the carrier wave generated by trapezoidal wave arranged in PDPWM, PODPWM, APODPWM and PSPWM are compared with the reference wave generated from the different reference signals. Figure 6(a) shows the generated gate waveforms and Figure 6(b) shows the voltage across the DC bus capacitor which are almost in balance condition.

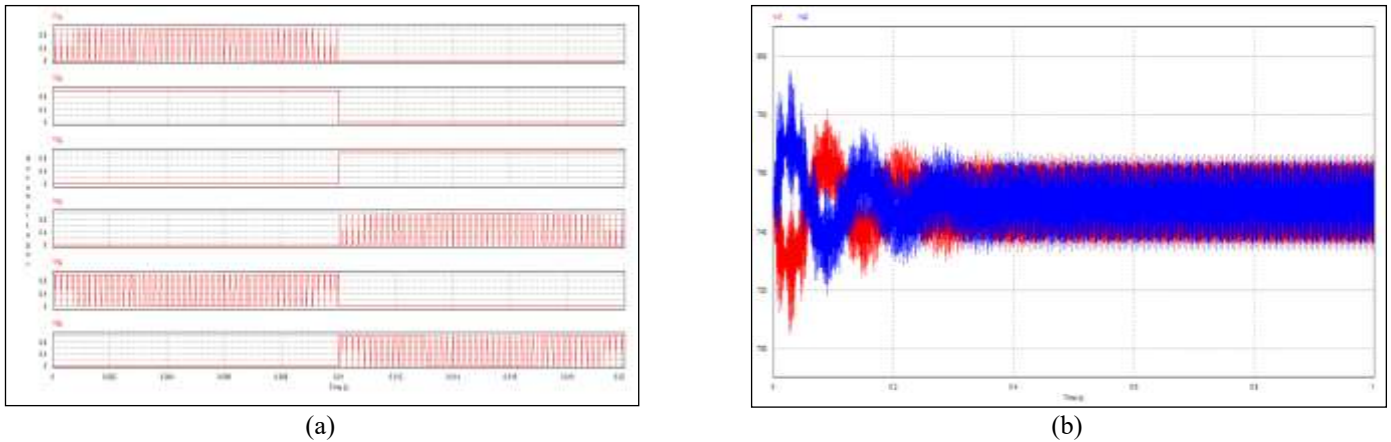


Figure 6: ANPC inverter (a) gate signals for switch Sa1 to Sa6 (b) Voltage across DC capacitor.

Source: Authors, (2026).

Comprehensive analyses for PWM1 to PWM4 gate pulses are carried out in order to validate the aforementioned proposed work. The findings are compared as the RMS value of output voltage, %THD, and the maximum voltage stress across the switching devices.

V.1 PWM1 FED ANPC INVERTER OUTPUT VOLTAGE, THD AND PEAK VOLTAGE ACROSS SWITCHING DEVICE

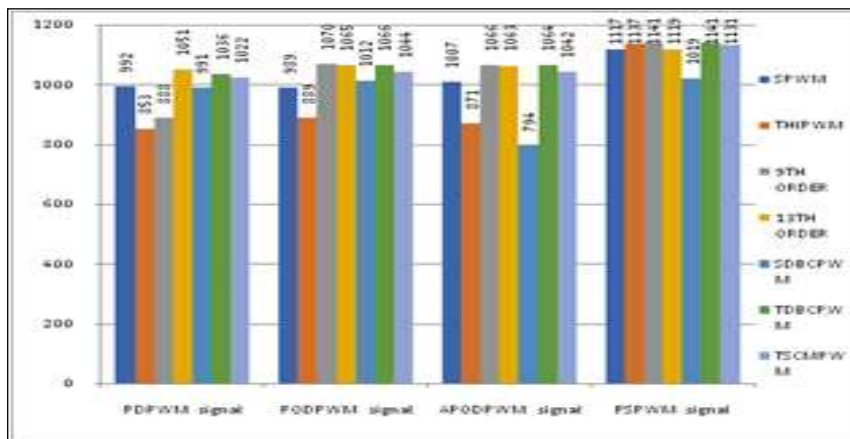


Figure 7: Comparison of RMS output voltages for PWM1.

Source: Authors, (2026).

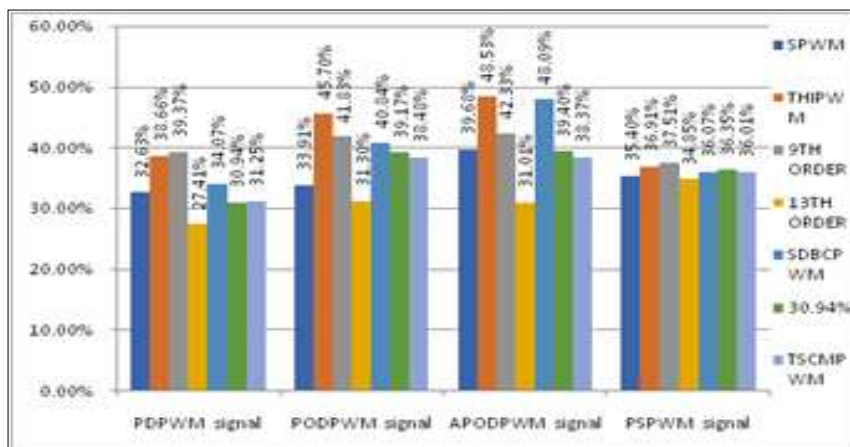


Figure 8: Comparison of RMS output voltages for PWM1.

Source: Authors, (2026).

Table 3: PWM1 fed Inverter Peak voltage across switch.

Reference waveform	Signal	Peak voltage across each IGBT(volt)					
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6
SPWM	PDPWM	887	878	870	909	871	879
	PODPWM	794	792	791	804	791	792
	APODPWM	854	804	790	804	791	804
	PSPWM	854	805	798	864	798	805
THIPWM	PDPWM	1018	958	939	1033	940	958
	PODPWM	985	920	921	983	922	920
	APODPWM	855	841	827	866	827	841
	PSPWM	1210	929	905	943	908	929
9 TH ORDER	PDPWM	1001	916	918	987	919	917
	PODPWM	860	824	784	803	787	824
	APODPWM	1057	872	842	914	845	872
	PSPWM	920	868	804	835	807	868
13 TH ORDER	PDPWM	943	882	890	944	891	882
	PODPWM	1017	912	872	895	875	912
	APODPWM	1085	946	894	898	898	947
	PSPWM	1294	1012	905	973	909	1012
SDBCPWM	PDPWM	855	817	787	821	789	817
	PODPWM	855	810	790	792	793	810
	APODPWM	841	821	814	846	814	821
	PSPWM	908	967	973	849	804	870
TDBCPWM	PDPWM	868	874	926	833	818	874
	PODPWM	954	865	858	944	858	865
	APODPWM	837	793	797	832	793	793
	PSPWM	1247	1409	1458	1104	933	1047
TSCMPWM	PDPWM	829	823	793	809	796	823
	PODPWM	859	825	794	815	797	825
	APODPWM	848	818	795	806	798	818
	PSPWM	908	860	800	837	800	860

Source: Authors, (2026).

From the given Figure 7, Figure 8 and Table 3 it can be seen that the lowest voltage THD 27.41% and rms voltage 1051V with voltage peak across each device obtained less then 1200V in PDPWM with reference signal taken as 13th order harmonic injection method. The highest rms voltage 1141V obtained when PSPWM technique is used in 9th order harmonic injection and TDBCPWM method but the voltage THD obtained are 37.51% and 36.53% respectively but the peak voltage of TDBCPWM fed reference signal crosses the 1200V.

V.2 PWM2 FED ANPC INVERTER OUTPUT VOLTAGE, THD AND PEAK VOLTAGE ACROSS SWITCHING DEVICE

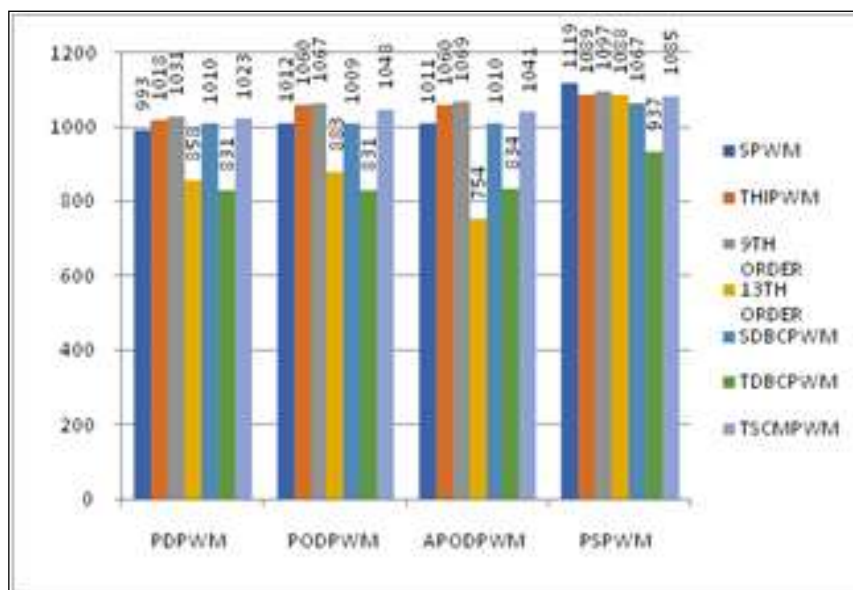


Figure 9: Comparison of RMS output voltages for PWM2.

Source: Authors, (2026).

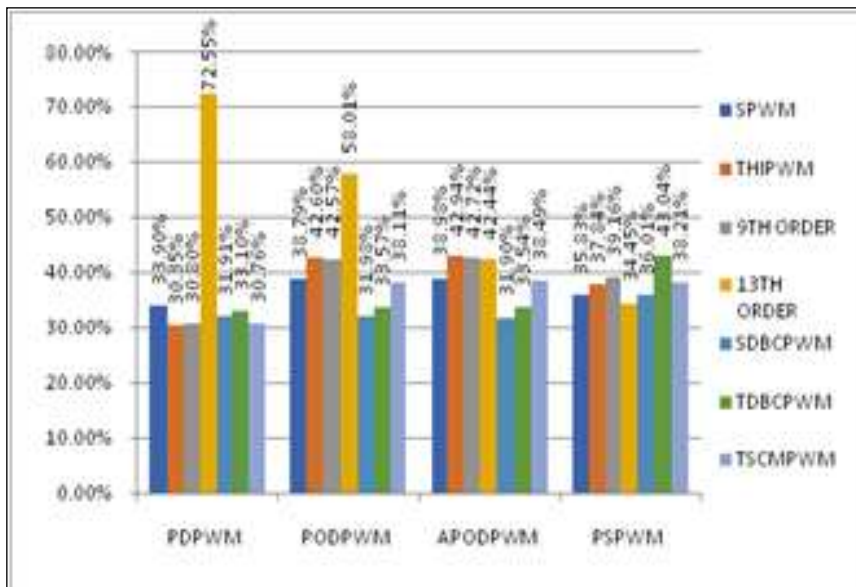


Figure 10: Comparison of %THD of output voltage for PWM2.
Source: Authors, (2026).

Table 4: PWM2 fed Inverter Peak voltage across switch.

Reference waveform	Signal	Peak voltage across each IGBT(volt)					
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6
SPWM	PDPWM	855	922	1441	832	807	867
	PODPWM	853	899	982	845	808	837
	APODPWM	854	835	1029	845	806	835
	PSPWM	915	991	1041	1059	790	794
THIPWM	PDPWM	790	791	776	798	779	791
	PODPWM	790	791	779	799	779	791
	APODPWM	790	790	778	798	778	790
	PSPWM	798	875	943	887	747	875
9 TH ORDER	PDPWM	786	783	768	797	770	783
	PODPWM	812	981	1022	811	789	789
	APODPWM	787	781	769	794	770	781
	PSPWM	953	1122	1306	1076	782	885
13 TH ORDER	PDPWM	797	787	1071	789	798	787
	PODPWM	823	803	1349	813	801	804
	APODPWM	793	788	1062	790	789	788
	PSPWM	783	1951	1183	884	775	980
SDBCPWM	PDPWM	834	978	1050	839	826	823
	PODPWM	831	1017	1074	833	819	822
	APODPWM	894	1192	1175	890	824	847
	PSPWM	737	1943	1897	899	762	1042
TDBCPWM	PDPWM	813	807	812	806	813	804
	PODPWM	915	857	1070	1086	855	858
	APODPWM	918	867	993	855	900	861
	PSPWM	830	1328	1053	960	678	1056
TSCMPWM	PDPWM	868	832	1383	893	836	832
	PODPWM	868	833	1398	892	820	833
	APODPWM	832	1388	1517	818	826	825
	PSPWM	945	2240	1322	1144	785	1052

Source: Authors, (2026).

From Figure 8, Figure 9 and Table 4 shows that lowest voltage THD obtained is 30.35% with carrier signal in PDPWM mode and reference signal in 3rd harmonic injection method with rms output voltage 1018V and the peak voltage across the entire switching device is less than 1200V. The highest rms voltage obtained by carrier signal in PSPWM carrier signal with SPWM type reference signal.

V.3 PWM3 FED ANPC INVERTER OUTPUT VOLTAGE, THD AND PEAK VOLTAGE ACROSS SWITCHING DEVICE

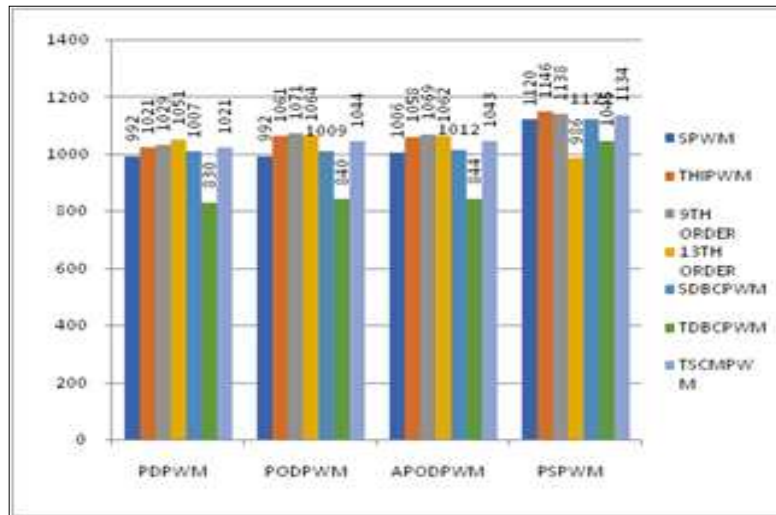


Figure 11: Comparison of RMS output voltage for PWM3.

Source: Authors, (2026).

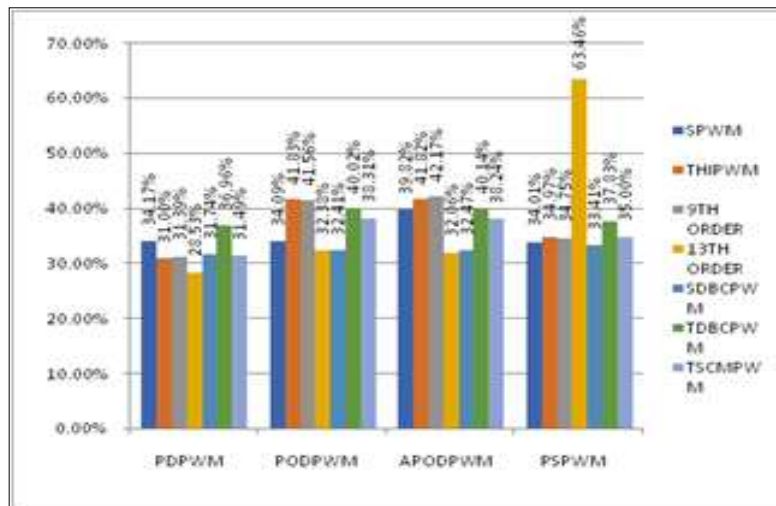


Figure 12: Comparison of %THD of output voltage for PWM3.

Source: Authors, (2026).

Table 5: PWM3 fed Inverter Peak voltage across switch.

Reference waveform	Signal	Peak voltage across each IGBT(volt)					
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6
SPWM	PDPWM	852	876	807	847	790	800
	PODPWM	852	876	808	847	789	800
	APODPWM	852	1005	896	837	790	804
	PSPWM	1219	801	1095	841	1098	801
THIPWM	PDPWM	846	867	811	842	801	816
	PODPWM	849	892	827	843	795	821
	APODPWM	845	1006	890	838	800	817
	PSPWM	1217	784	1081	832	1084	784
9 TH ORDER	PDPWM	846	1027	846	847	795	823
	PODPWM	836	927	845	846	789	824
	APODPWM	847	1025	899	840	796	819
	PSPWM	1218	796	1091	841	1094	796
13 TH ORDER	PDPWM	850	987	853	863	800	818
	PODPWM	836	928	844	862	802	818
	APODPWM	850	1022	932	848	799	821
	PSPWM	1219	774	1086	818	1089	774
SDBC PWM	PDPWM	934	1314	1226	928	865	891
	PODPWM	1083	1459	1194	1047	893	905
	APODPWM	1054	1806	1411	1020	883	920

	PSPWM	1227	926	1110	1070	1114	927
TDBCPWM	PDPWM	895	1202	1304	871	906	884
	PODPWM	1046	1329	1115	959	919	935
	APODPWM	899	1093	1137	866	865	881
	PSPWM	1224	888	1106	1031	1110	888
TSCMPWM	PDPWM	849	912	884	850	796	823
	PODPWM	849	1081	935	851	797	825
	APODPWM	849	909	835	839	797	817
	PSPWM	1216	803	1094	837	1097	803

Source: Authors, (2026).

From Figure 11, Figure 12 and Table 5 the lowest voltage THD obtained is 28.53% with carrier signal in PDPWM mode and reference signal in 13th order harmonic injection method with rms output voltage 1051V and the peak voltage across the entire switching device is less than 1200V. The highest rms voltage is 1051V with carrier signal in PSPWM and reference signal in 3rd harmonic injection method with voltage THD 34.97% but the peak voltage across switching device Sa1 crosses the 1200V.

V.4 PWM4 FED ANPC INVERTER OUTPUT VOLTAGE, THD AND PEAK VOLTAGE ACROSS SWITCHING DEVICE

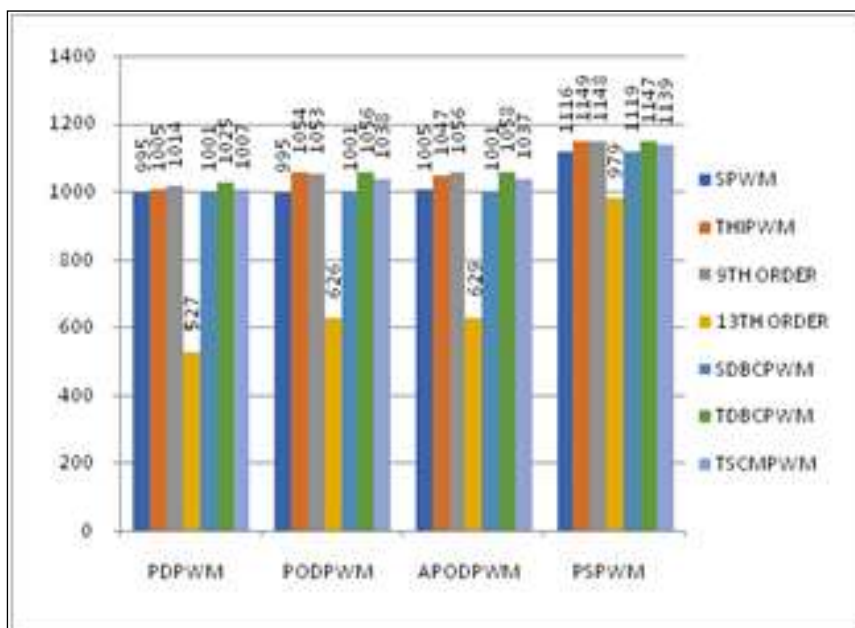


Figure 13: Comparison of RMS output voltages for PWM4.

Source: Authors, (2026).

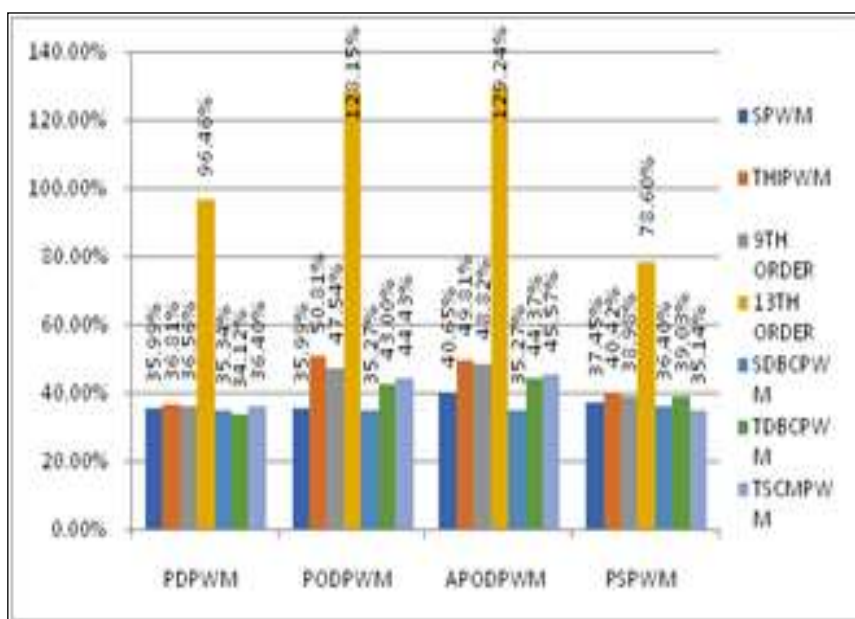


Figure 14: Comparison of %THD of output voltage for PWM4.

Source: Authors, (2026).

Table 6: PWM2 fed Inverter Peak voltage across switch.

Reference waveform	Signal	Peak voltage across each IGBT(volt)					
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6
SPWM	PDPWM	1112	1780	1737	1101	1097	1098
	PODPWM	1112	1780	1737	1101	1097	1098
	APODPWM	1112	1846	1741	1101	1099	1097
	PSPWM	1084	1702	1738	1083	1071	1076
THIPWM	PDPWM	1096	1741	1675	1098	1123	1087
	PODPWM	1102	1771	1667	1203	1086	1092
	APODPWM	1100	1687	1694	1093	1081	1088
	PSPWM	1079	1708	1710	¹ 190	1058	1068
9 TH ORDER	PDPWM	1093	1642	1654	1119	1081	1084
	PODPWM	1090	1667	1704	1091	1077	1079
	APODPWM	1096	1722	1702	1115	1077	1092
	PSPWM	1075	1708	1654	¹⁰ 95	1066	1075
13 TH ORDER	PDPWM	1085	1688	1733	1202	799	827
	PODPWM	1081	1690	1761	1200	1081	1100
	APODPWM	1085	1690	1733	1099	1082	1099
	PSPWM	1064	1708	1928	1079	1081	1091
SDBCPWM	PDPWM	1097	1678	1744	1094	1099	1099
	PODPWM	1101	2005	1667	1096	1096	1096
	APODPWM	1096	2085	1739	1100	1095	1097
	PSPWM	1061	1700	1751	1069	1068	1150
TDBCPWM	PDPWM	1073	1676	1812	1214	1140	1127
	PODPWM	1209	1705	1733	1214	1093	1093
	APODPWM	1206	1699	1705	1218	1096	1087
	PSPWM	1065	1713	1730	1081	1070	1082
TSCMPWM	PDPWM	1108	1770	1804	1123	1133	1137
	PODPWM	1102	1678	1748	1106	1087	1095
	APODPWM	1104	1696	1743	1110	1088	1095
	PSPWM	1229	935	1238	1063	1113	935

Source: Authors, (2026).

From Figure 13, Figure 14 and Table 6 the lowest voltage THD obtained is 34.12% with carrier signal in PDPWM mode and reference signal in TDBCPWM method with rms output voltage 1025V and the peak voltage across the switching device Sa2, Sa3 and Sa4 crosses the 1200V.

VI. INTERPREATION OF SIMULATION RESULTS

From the simulation results for all PWM combinations (PWM1-PWM4) using two main metrics: % THD and the peak voltage stress on each switching device (Sa1-Sa6). The switching device selected having the rating of 1200V peak so the peak voltage can't exceed the IGBTs' 1200V rating.

VI.1 ANALYSIS OF THD

The results illustrate the comparative THD performance of various PWM techniques under different modulation strategies. The finding evident that harmonic injected and carrier based PWM techniques exhibit relatively lower THD values compared to conventional SPWM. In particular, THIPWM and 9th-order harmonic injection methods consistently demonstrate improved harmonic suppression. Among multicarrier strategies, PDPWM and APODPWM show comparatively better performance, with THD values generally remaining in the range of 30% to 40% for most modulation techniques. This indicates their superior ability to distribute switching harmonics and reduce waveform distortion. The THD levels of SDBCPWM, TDBCPWM, and TSCPWM approaches are moderate and constant, suggesting balanced performance across various modulation schemes. PSPWM is less suitable for applications needing high power quality because it often exhibits somewhat greater distortion than PDPWM and APODPWM. The results obtained support the notion that higher THD performance can be achieved by combining PDPWM and APODPWM with THIPWM or 9th-order harmonic injection. These combinations successfully reduce distortion and enhance the quality of the output voltage. For high-performance power electronic applications where lower harmonic content and increased efficiency are crucial, they are so advised.

VI.2 ANALYSIS OF MAXIMUM VOLTAGE STREE ACROSS THE SWITCHING DEVICES

The maximum voltage stress on the IGBTs is an important measure of reliability. Results show that the ideal blocking voltage is 750V (half of 1500V), but the actual measured peak voltage was often higher than this because of switching transients and parasitic oscillations. The Phase-Shifted PWM (PSPWM) method often caused peak voltages to exceed 1200V, especially when used with high-frequency reference injections like the 13th order method.

The carriers for the different levels are phase-shifted in PSPWM. This can make the upper and lower switches in a phase leg switch quickly or in a way that makes the di/dt in the commutation loop very high. The rapid change in current, along with the parasitic inductance ($V = L * di/dt$), causes a large voltage spike across the switches when they are turned off. Also, the energy stored in the inductance resonates with the device capacitance, which makes a high-frequency ringing waveform on top of the DC blocking voltage. The peak of this ringing waveform typically exceeds the 1200 V limit, as shown by results like PSPWM with 13th order (1294V). PDPWM and PODPWM make switching events happen at the same time more often. The commutation paths are easier to predict and usually have shorter or less disruptive commutation loop geometries. This makes the di/dt and the resulting voltage overshoot as small as possible. Ringing is still observed under the 30 nH/120 nH parasitic inductance conditions, but its peak amplitude is usually kept within a safer range below the device rating. High voltage stress can also happen with bus-clamping methods like SDBCPWM and TDBCPWM. By clamping a phase to the bus for 60 or 30 degrees, the switching events occur primarily at the beginning and end of the clamping period. This can cause multiple devices to switch at the same time or very close to the same time, which can create complicated, high-energy commutation loops that make voltage spikes worse, as seen in TDBCPWM with PSPWM (1458V).

VII. CONCLUSIONS

A comparative analysis of the components used for various topologies for a three-level inverter used in a 1500V DC bus system was conducted, and the results show that the ANPC inverter offers more benefits than the other topologies. Several reference signals were compared for a three-level ANPC inverter using PSIM software, and the simulation was run using a trapezoidal carrier signal with different phase shifts. These PWM techniques were compared based on the peak voltage across the switching device, the rms value of the output phase voltage, and the percentage THD value of the output phase voltage to analyze the performance of the three-level ANPC inverter. The simulation results demonstrate that the maximum rms voltage can be reached in PSPWM mode and that the voltage THD is reduced when the carrier signal operates in PDPWM mode. The %THD value was found to be within a moderate range by further analyzing the PWM3 and PWM4 types of pulse generation; however, the peak voltage across the switching device surpasses the maximum device rating of 1200V. With a trapezoidal carrier signal in PDPWM mode, a modulation index of 1, and a switching frequency of 5 kHz, the lowest voltage %THD was attained using the PWM1 and PWM2 approaches.

VIII. AUTHOR'S CONTRIBUTION

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Investigation: Miteshkumar N Priyadarshi, Sandeep Chakravorty.

Discussion of results: Miteshkumar N Priyadarshi, Sandeep Chakravorty.

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Writing – Review and Editing: Miteshkumar N Priyadarshi, Sandeep Chakravorty.

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Supervision: Miteshkumar N Priyadarshi, Sandeep Chakravorty.

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