

SYNERGISTIC HYBRID GDI–CNTFET ARCHITECTURE FOR LOW-POWER AND AREA-OPTIMIZED NANOSCALE VLSI CIRCUITS

Jayakrishna Padala¹, Kishore Kumar Kamarajugadda², Pavani Movva³

¹Research Scholar, Department of ECE, FoET, The ICFAI University, Raipur, India.

²Professor, Department of ECE, FoET, The ICFAI University, Raipur, India.

³Professor, Department of ECE, Nalla Malla Reddy Engineering College, Hyderabad, India.

¹<https://orcid.org/0009-0009-9498-2597>, ²<https://orcid.org/0000-0002-6286-1186>, ³<https://orcid.org/0000-0003-1987-9185>

Email: pjayakrishnachary@gmail.com, jayakrishnap.phd2023@iuraipur.edu.in, kishorekamarajugadda@gmail.com, drmovvapavani@gmail.com

ARTICLE INFO

Article History

Received: February 26, 2026

Reviewed: June 11, 2026

Accepted: July 11, 2026

Published: July 31, 2026

Keywords:

Hybrid GDI–CNTFET,
Carbon NanoTube Field Effect
Transistor,
Gate Diffusion Input,
Low-Power VLSI,
Area-Efficient Design,
Cadence Virtuoso Tool,
Nanoscale Technology,
Digital Circuits.

ABSTRACT

As CMOS technology continues to expand to a deep sub-micron scale, standard designs are confronted with many challenges in terms of energy dissipation, leakage currents and area. Although GDI logic minimizes the number of transistors and CNTFET offers improved transport performance, it is on its own that it provides optimal performance. This paper proposes a hybrid design methodology for GDI and CNTFETs combining the structural compactness of GDI with the near ballistic electrical characteristics of 32 nm CNTFETs. The complete digital building block library, including basic logic gates, arithmetic units (half-adder, full-adder), data-routing circuits (multiplexer, encoder, decoder) and sequencing elements (D and Jk flip-flops) have been developed in the Cadence tool based on Stanford 32 nm CNTFET model. Transient, DC and AC analysis confirm full swing logic and high frequency response. The simulation results indicate that the proposed hybrid architecture achieves a reduction of 40-70% in power and 25-55% in silicon area compared to conventional CMOS and standalone GDI, CNTFET reference products, and is a much improved Power-Delay Product. These findings, together with the significantly improved PDP, make the GDI-CNTFET hybrid framework a viable and scalable solution for energy-efficient nano-electronic systems.



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I. INTRODUCTION

The relentless pursuit of Moore's Law [1] has pushed integrated circuit (IC) technology down to the deep sub-micron and nanometer scale, and this has led to the need for low-power, high-speed and area-efficient VLSI systems [2]. This is particularly important for the emerging areas of Internet of Things (IoT), implantable biomedical sensors and edge computing. However, bulk CMOS has significant physical scaling limitations [3], such as leakage current, short-channel effects and threshold voltage variations, which cause performance and reliability problems. To overcome these constraints, researchers have investigated both architectural and device-level innovations. Gate Diffusion Input (GDI) logic is a promising approach at the architectural level to minimize the number of transistors and the switching activity [4], which can be implemented with fewer devices than conventional CMOS [5], leading to lower dynamic power consumption and lower silicon area, but suffers from intrinsic drawbacks, such as reduced output voltage swings and decreased noise margins, which cause the cascaded high-performance systems to become unstable [6]. Simultaneously, Carbon Nanotube Field-Effect Transistors (CNTFETs) have gained prominence as a robust post-CMOS successor. CNTFETs offer extraordinary electrical properties [7], including near-ballistic carrier transport, symmetric threshold voltages, and superior electrostatic control due to their unique geometry. While CNTFETs inherently address the leakage and performance issues [8] of silicon, implementing them using traditional CMOS-like topologies often results in redundant device counts and increased wiring complexity. A critical analysis of current literature [9] reveals a fragmented research landscape: GDI logic is primarily studied for area optimization [10], while CNTFET technology is investigated for power-delay performance [11]. There is a notable absence of a unified hybrid design framework that merges the architectural compactness of GDI with the superior material physics of CNTFETs.

While our previous research established the independent merits of these technologies, this work proposes a novel Hybrid GDI–CNTFET methodology. This co-design strategy leverages the reduced-transistor topology of GDI [12] while utilizing the high-mobility, low-leakage characteristics of CNTFETs [13] to mitigate the traditional GDI "voltage drop" problem through better drive strength. The main objective of this research work is to go beyond the isolated optimization as implied in the graphical version of abstract shown in Figure 1. We implemented this hybrid technique to a set of digital circuits and performed a comprehensive performance evaluation on transistor count, power dissipation, propagation delay, and the Power–Delay Product (PDP). Benchmarking results against conventional CMOS, stand-alone GDI, and CNTFET designs demonstrate that the proposed hybrid approach presents a superior Pareto-optimal solution for next-generation VLSI systems.

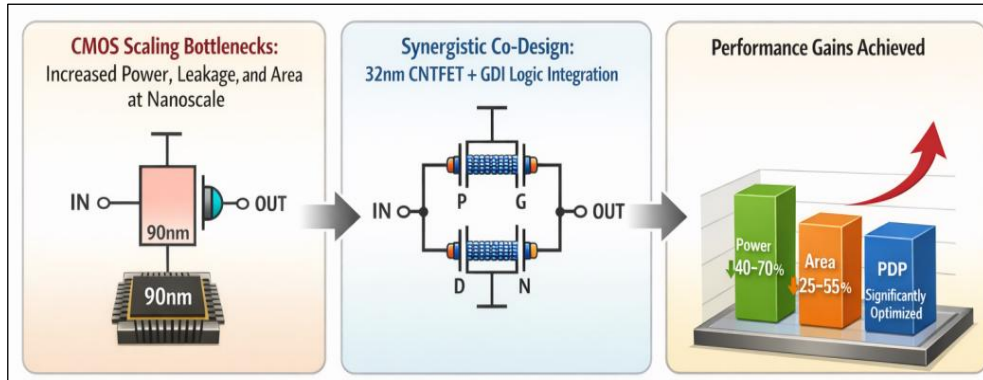


Figure 1: Graphical version of abstract.

Source: Authors, (2026).

The remainder of this paper follows the background and literature surveys conducted for GDI and CNTFET in section-2; section-3 details the proposed hybrid methodology; section-4 describes the implementation of digital circuits with proposed methodology using the Cadence Virtuoso simulation environment; section-5 discusses the results and benchmarking; and section-6 concludes with a future research direction.

II. BACKGROUND AND LITERATURE SURVEY

This section provides the technical basis for research, starting with the introduction of Gate-Diffusion-Input logic and Carbon NanoTube Field Effect Transistor technology. Although GDI [14] simplifies the process of minimizing the number of transistors and power dissipation, its integration into high-performance systems is typically limited by signal degradation. On the other hand, although CNTFETs [15] are the ideal for post-silicon scaling because of their higher carrier mobility, their usage in standard logic topologies is limited. The literature survey [16] performed revealed major design constraints in contemporary designs, particularly in voltage swing restoration and noise immunity. By addressing these limitations [17], the motivation for the proposed Hybrid GDI–CNTFET methodology, a design paradigm engineered to harness the high-speed ballistic transport of carbon nanotubes to overcome the inherent architectural weaknesses of traditional GDI logic.

II.1 GATE DIFFUSION INPUT (GDI) LOGIC:

GDI logic is a low-power circuit design technique [18] that reduces the number of transistors and silicon area when compared to standard CMOS logic. While in standard CMOS, the source terminals of PMOS and NMOS transistors are always connected to the power rails, in the GDI cell, multiple input signals can be applied to the gate, source, and drain terminals, which can be used to realize several logic functions using fewer transistors, leading to reduced area and lower dynamic power consumption. It has been proven that GDI logic can be used to design compact digital circuits such as adders, multiplexers, encoders, decoders and flip-flops with significant reductions in the area and power dissipation compared to CMOS designs.

II.2 CARBON NANOTUBE FIELD-EFFECT TRANSISTOR (CNTFET) TECHNOLOGY:

CNTFETs have been proposed as a possible alternative to conventional CMOS devices for nano-scale VLSI systems [19], because of their high-speed operation with improved energy efficiency, low off-state leakage and symmetric threshold voltages, but existing CNTFET-based designs mainly utilize CMOS logic styles, which often lead to a higher transistor count for complex logic functions and increases the silicon area & routing complexity.

II.3 LITERATURE SURVEY ON LOW-POWER AND AREA-EFFICIENT DESIGNS:

While research in alternative logic styles and emerging device technologies to reduce power dissipation and area in VLSI circuits has been widely studied [20], research on GDI logic has primarily focused on minimizing the number of transistors and area, and research on CNTFETs has primarily focused on improving power and performance at advanced technology nodes [21]. Comparative analyses between CMOS, GDI, and CNTFET implementations have shown that no single approach optimizes power, delay, and area simultaneously. There are a few works that have investigated hybrid logic styles, such as combining pass-transistor logic [22] with CMOS or using CNTFETs in standard logic configurations.

But to the best of our knowledge, no systematic investigation [23] has been performed into a hybrid design methodology that incorporates GDI logic topology with CNTFET technology in the same design.

II.4 MOTIVATION FOR THE PROPOSED HYBRID GDI–CNTFET METHODOLOGY:

Existing research and our prior research work validate that GDI logic and CNTFET technology complement each other [24], with GDI logic reducing area through minimal transistor usage, while CNTFETs provide improved power efficiency, improved voltage swing, and high-speed operation. However, current design approaches optimize these benefits independently, and so they do not achieve concurrent improvements in power and area. This work proposes a Hybrid GDI–CNTFET methodology, which aims to leverage the advantages of GDI circuits (such as low power consumption, minimum delay, and low silicon area) while overcoming the voltage swing and noise margin issues of the CMOS-based GDI circuits [25] by integrating GDI-based logic structures with CNTFET devices. This approach serves as the basis for circuit implementations and performance evaluations presented in the subsequent sections.

III. DEVICE MODELLING AND PROPOSED METHODOLOGY

The design and evaluation of digital circuits, are carried out using an integrated framework that combines the logic-level compactness of Gate Diffusion Input (GDI) with the device-level advantages of Carbon Nanotube Field-Effect Transistors (CNTFETs). This section describes the CNTFET device model employed [26], the GDI logic cell structure [27], the proposed Hybrid GDI–CNTFET design technique, and the overall methodology adopted for circuit implementation and performance evaluation as shown in Figure 2.

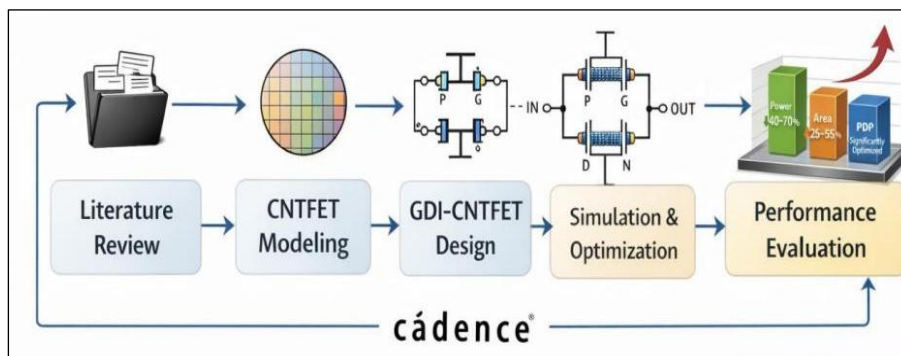


Figure 2: Methodology for Hybrid GDI-CNTFET circuits implemented.
Source: Authors, (2026).

III.1 CNTFET DEVICE MODELLING:

For all the circuits discussed, the Stanford CNTFET compact model [28] is used to accurately simulate carbon nanotube-based devices at the nano-meter technology nodes. The model includes the key physical phenomena, such as near-ballistic carrier transport, quantum confinement, and electrostatic control, which are essential for predicting CNTFET behaviour in digital circuits. Device parameters that are critical for the CNTFET model are the carbon nanotube diameter, which controls the bandgap energy and threshold voltage, the channel length, which impacts carrier transport and switching speed, and the inter-tube pitch, which impacts the device density. Other parameters, such as the number of nanotubes per device, gate work function and chirality vector, are selected to optimise the trade-off between power consumption and the propagation time. Simulations were performed using the Cadence Virtuoso Custom IC Design Platform with the Spectre simulator, enabling accurate transient, DC, and AC analyses at the 32nm technology node. The near-ballistic transport characteristics of CNTFETs significantly reduce scattering effects, resulting in enhanced switching speed and lower power dissipation compared to conventional CMOS devices.

III.2 GDI LOGIC CELL MODELLING:

The proposed hybrid design uses Gate Diffusion Input (GDI) logic [29], which is a logic foundation that requires the use of a minimal number of transistors to implement a variety of logic functions, including NAND, OR, XOR, multiplexers, flip-flops, and arithmetic blocks. GDI logic reduces the number of transistors and switching activity and therefore reduces silicon area and dynamic power consumption compared to CMOS logic. But CMOS-based GDI implementations suffer from threshold voltage loss, degraded output swing, and reduced noise margins, especially when the bulk is fixed and the inputs are source driven, which limits the scalability and robustness of CMOS-GDI designs.

III.3 HYBRID GDI–CNTFET DESIGN TECHNIQUE:

To address the limitations of CMOS-based GDI logic while maintaining its area efficiency, this research work presents a Hybrid GDI–CNTFET design technique, in which conventional PMOS and NMOS devices in GDI cells are replaced with p-type and n-type CNTFETs [30], respectively. This hybridization ensures several benefits as, CNTFETs have symmetric threshold voltages and better electrostatic control, which allows them to operate with full swing even in source-driven GDI configurations, eliminating the threshold voltage degradation and output swing loss in CMOS-GDI circuits.

Moreover, CNTFETs have intrinsically low leakage current and superior subthreshold characteristics, leading to lower static power consumption. Because the GDI topology retains a minimal transistor count, the hybrid approach preserves the area efficiency while improving the electrical performance. The proposed Hybrid GDI–CNTFET technique [31] thus enables simultaneous optimization of power, delay, and area, addressing the primary limitations of GDI-only and CNTFET-only implementations.

III.4 DESIGN FLOW AND EVALUATION METHODOLOGY:

The complete design and evaluation process followed in this research is summarized below:

1. Adoption of the Stanford CNTFET compact model and GDI logic topology.
2. Mapping Boolean functions onto optimized GDI structures and replacing CMOS devices with CNTFET equivalents.
3. Design of digital circuits such as logic gates, XOR, half adder, full adder, multiplexer, encoder, decoder, and flipflops using hybrid GDI–CNTFET cells in Cadence Virtuoso tool.
4. Performing transient analysis to evaluate switching behavior, DC analysis to obtain voltage transfer characteristics, and AC analysis to study frequency response and stability.
5. Measurement of power consumption, propagation delay, output voltage swing, noise margin, and power–delay product (PDP).
6. Performance comparison of proposed hybrid circuits with conventional CMOS, GDI-only, and CNTFET-only implementations in terms of power, delay, PDP, and transistor count.

IV. HYBRID CIRCUIT DESIGN AND IMPLEMENTATION

This section presents design, operational principles, and performance benefits of proposed Hybrid GDI–CNTFET circuits, with emphasis on digital building blocks [32] like 2×1 multiplexer, XOR gate, full adder and other combinational and sequential circuits [33]. These circuits are selected because they form the core of arithmetic and data-path units and effectively demonstrate the ability of the hybrid methodology to achieve simultaneous power, delay, and area optimization. In the proposed approach, conventional NMOS and PMOS devices used in GDI logic are replaced with n-type and p-type CNTFETs, respectively. This integration preserves the compact topology of GDI logic while leveraging the near-ballistic transport, symmetric threshold voltages, and low leakage characteristics of CNTFET technology. All circuits are implemented and evaluated using the Cadence Virtuoso platform with the Stanford 32 nm CNTFET model.

IV.1 HYBRID XOR GATE:

The Hybrid XOR gate is implemented using conventional CMOS, which naturally realizes the Boolean expressions: $F = A'B + AB'$. The hybrid XOR gate requires only four CNTFET devices (two p-type and two n-type), which is significantly fewer than the 12 transistors required in CMOS XOR implementations and fewer than CNTFET-based XOR designs as shown in Figure 3a and 3b.

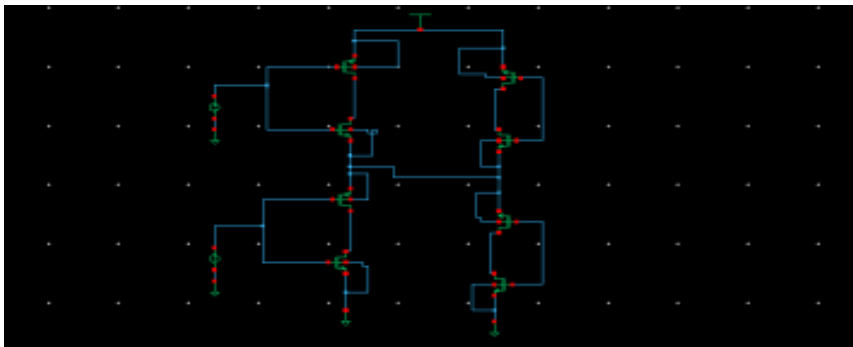


Figure 3a: Schematic of XOR gate using Conventional CMOS technology.
Source: Authors, (2026).

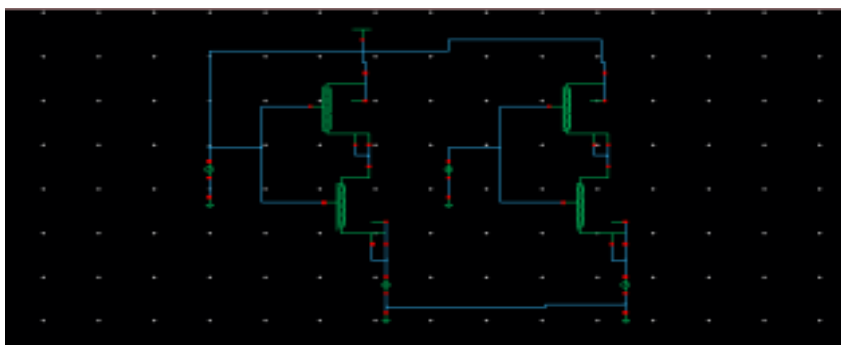


Figure 3b: Schematic of XOR gate using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

By replacing CMOS devices with CNTFETs, the hybrid XOR gate achieves full-swing output operation, indicated in Figure 3c eliminating the threshold voltage loss typically observed in CMOS-based GDI circuits. The near-ballistic transport of carriers in CNTFETs results in high switching speed and reduced propagation delay, while the minimal transistor count leads to lower parasitic capacitances and reduced dynamic power consumption.

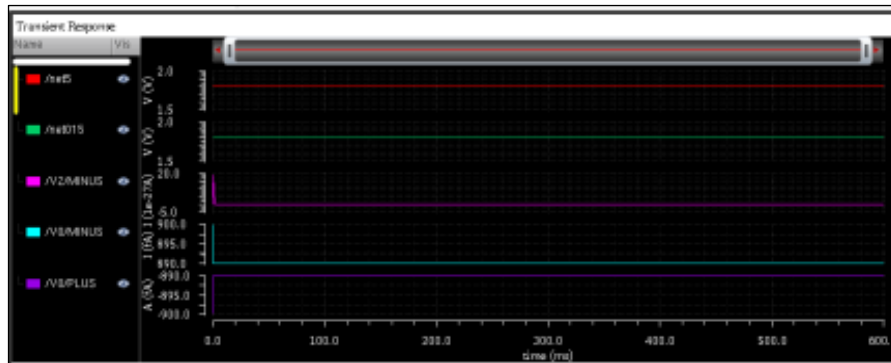


Figure 3c: Transient response of XOR gate using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

Simulation results indicate hybrid XOR gate offers substantial improvement in power–delay product, making it an efficient for arithmetic circuits and low-power digital systems.

IV.2 HYBRID 2×1 MULTIPLEXER:

The 2×1 multiplexer is implemented using a single GDI cell, where the select line controls gate terminal, and the data inputs are applied to source terminals. This configuration enables the realization of multiplexer function using only two CNTFET devices, representing a drastic reduction compared to CMOS implementations that require 6–8 transistors as represented in Figure 4a and 4b.

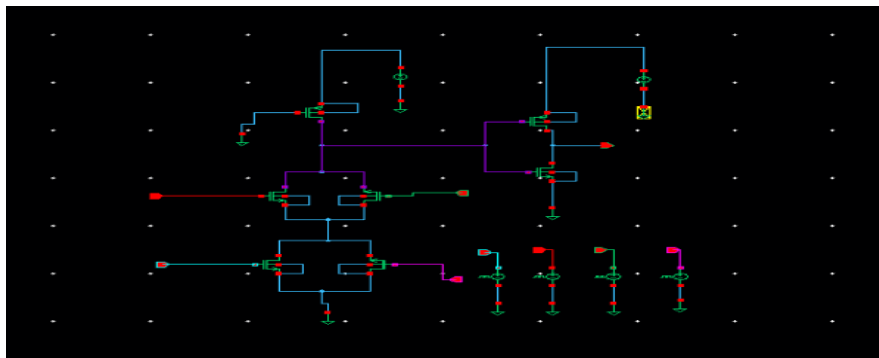


Figure 4a: Schematic of 2x1 multiplexer using Conventional CMOS technology.
Source: Authors, (2026).

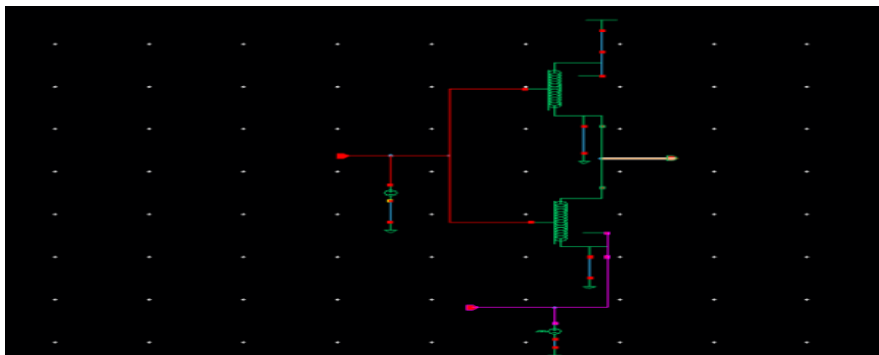


Figure 4b: Schematic of 2x1 multiplexer using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

In CMOS-based GDI multiplexers, incomplete voltage swing and degraded noise margins are common due to threshold voltage loss. In contrast, the hybrid GDI–CNTFET multiplexer achieves full-swing output across all input combinations, owing to the symmetric threshold voltages and superior electrostatic control of CNTFET devices, as shown in Figures (4- c,d,e,f,g,h).

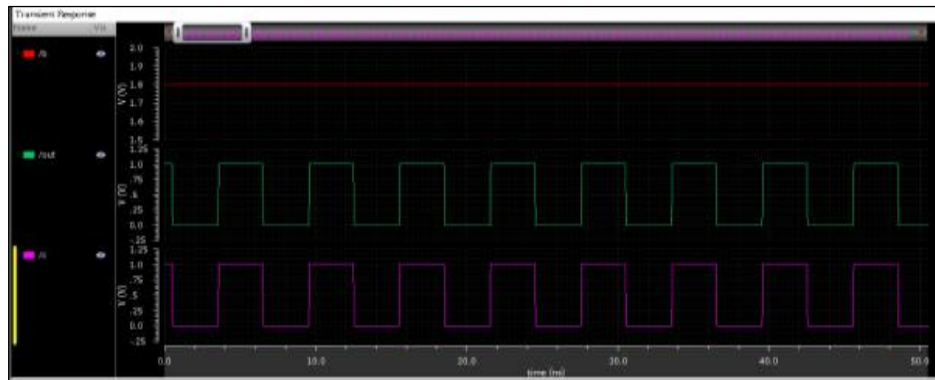


Figure 4c: Transient response of 2x1 multiplexer using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

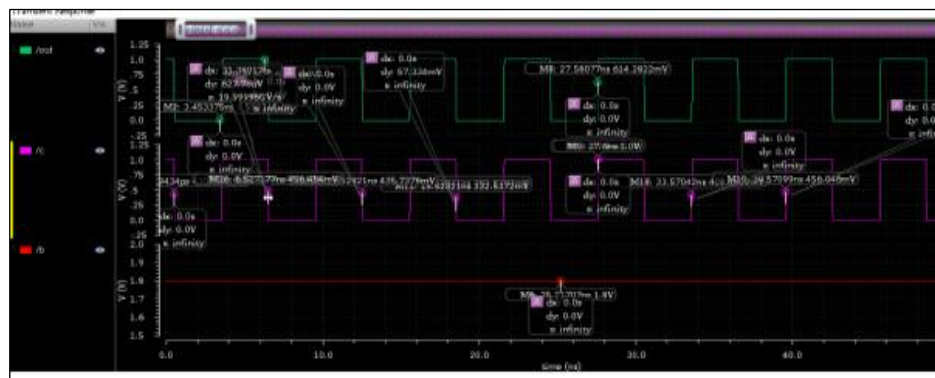


Figure 4d: Delay response of 2x1 multiplexer using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

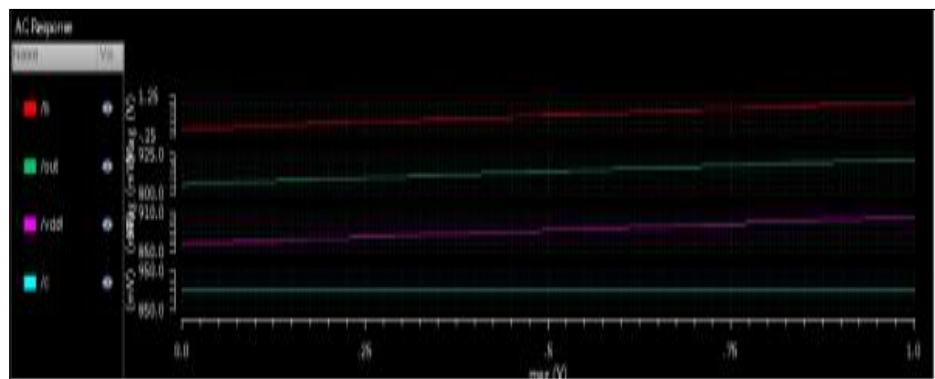


Figure 4e: AC response of 2x1 multiplexer using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

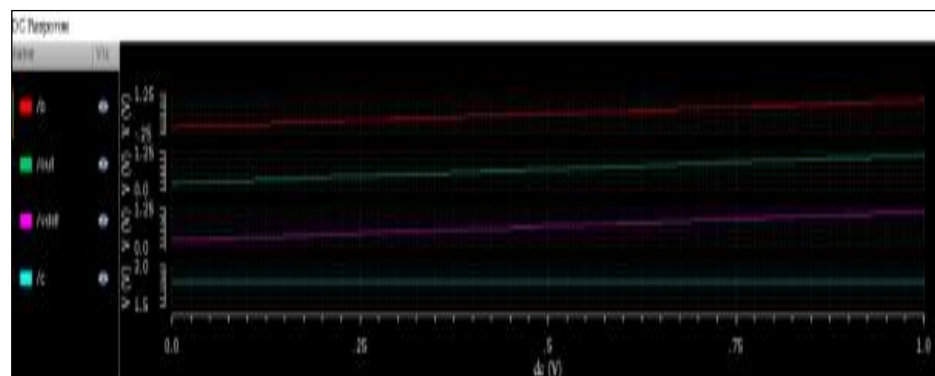


Figure 4f: DC response of 2x1 multiplexer using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

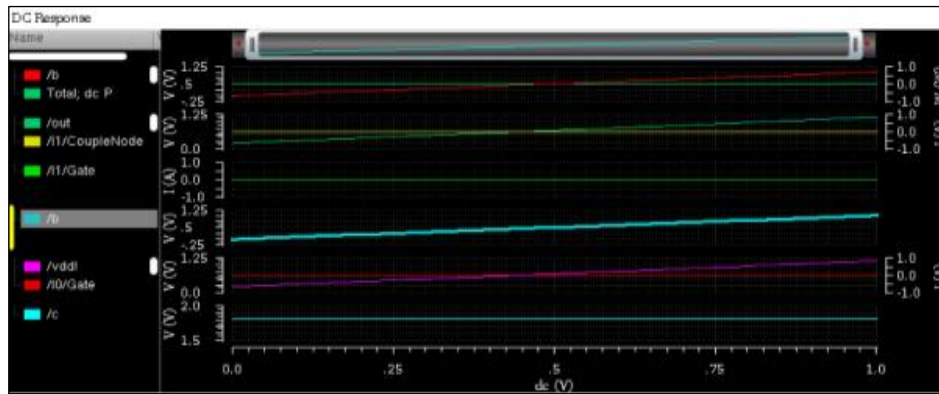


Figure 4g: Power analysis of 2x1 multiplexer using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

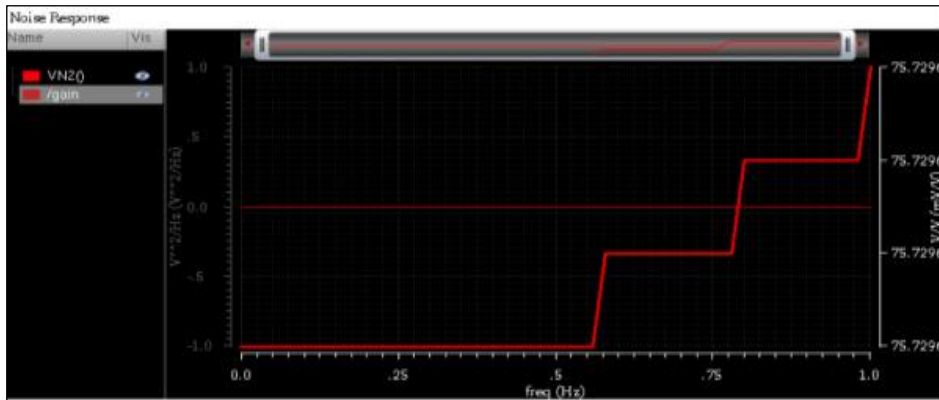


Figure 4h: Noise response of 2x1 multiplexer using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

The reduced device count and low parasitic capacitance contribute to lower switching power and faster response time, making the hybrid multiplexer well suited for high-speed data routing and selection operations in arithmetic and logic units.

IV.3 HYBRID FULL ADDER:

Hybrid Full-Adder is the most vital circuit used to validate the effectiveness of the proposed methodology, as it integrates both XOR and multiplexer logic within a single arithmetic unit. The full-adder is implemented using sum and carry blocks. This architecture reduces the transistor count, ensuring full-swing logic operation and functionality.

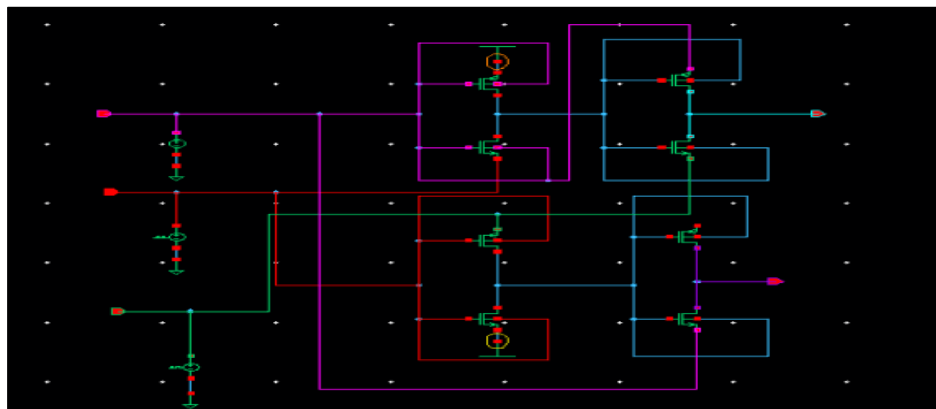


Figure 5a: Schematic of Full-adder using conventional CMOS technology.
Source: Authors, (2026).

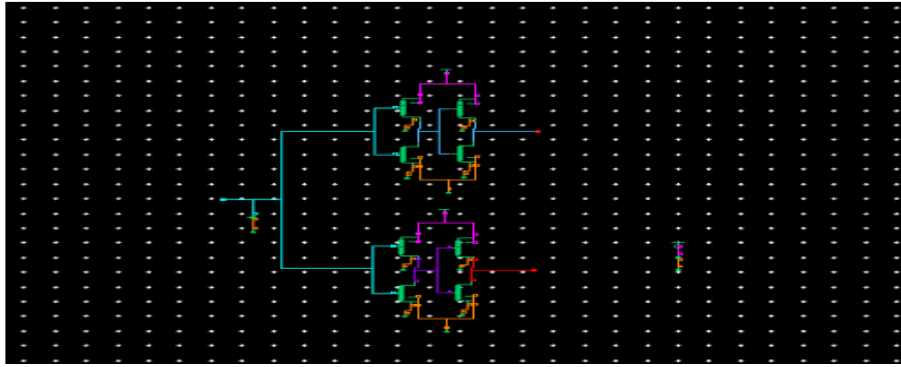


Figure 5b: Schematic of Full-adder using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

The proposed Hybrid GDI-CNTFET Full Adder requires only 6–8 CNTFET devices, compared to 28 transistors in CMOS, 10 transistors in conventional GDI, and approximately 18–20 devices in CNTFET designs as shown in Figure 5a and 5b. This significant reduction in device count directly translates into lower silicon area and reduced parasitic capacitances.

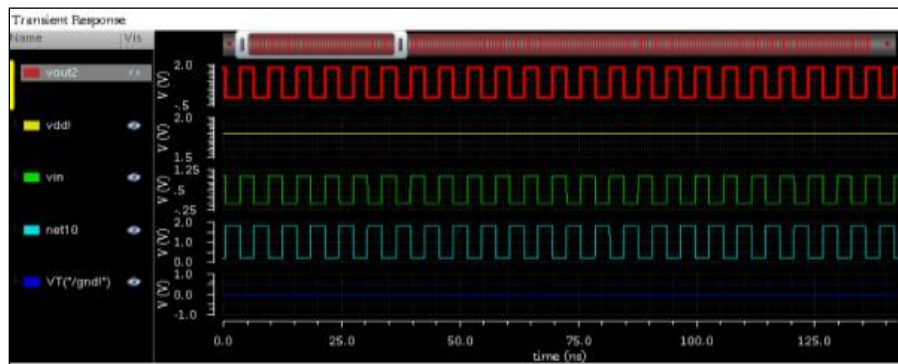


Figure 5c: Transient response of full-adder using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

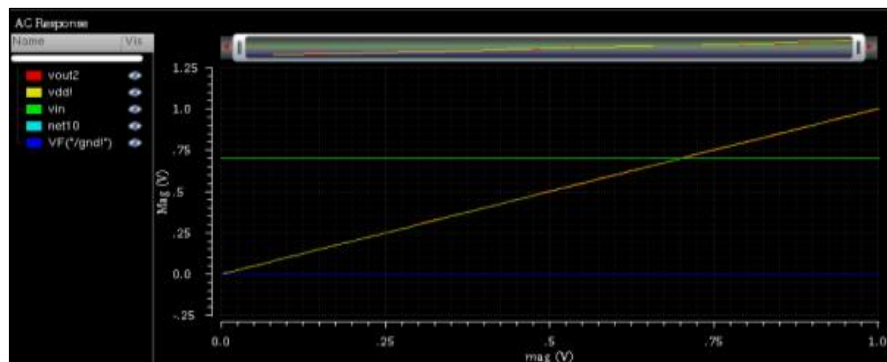


Figure 5d: AC response of full-adder using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

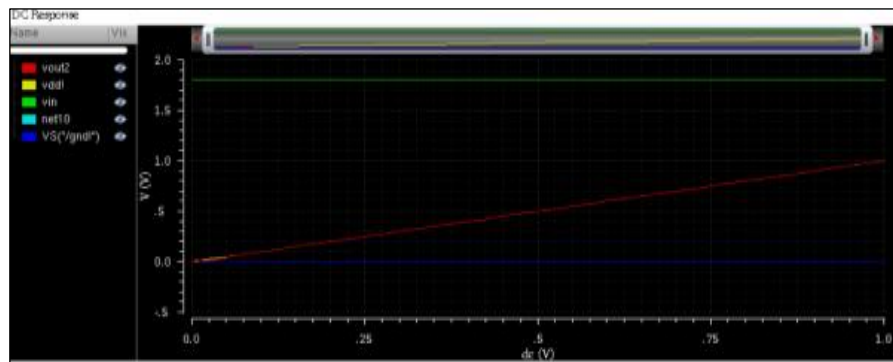


Figure 5e: DC response of full-adder using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

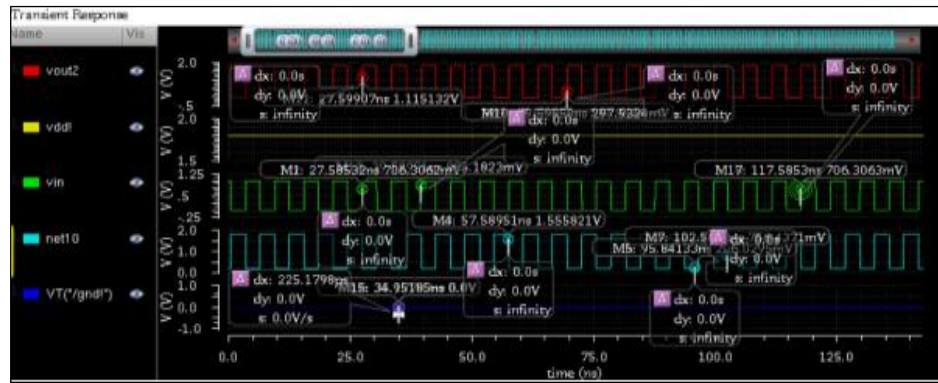


Figure 5f: Delay analysis of full-adder using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

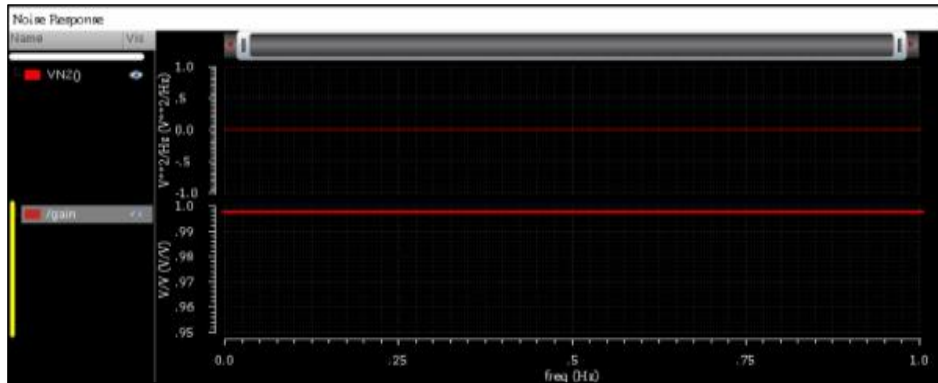


Figure 5g: Noise response of full-adder using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

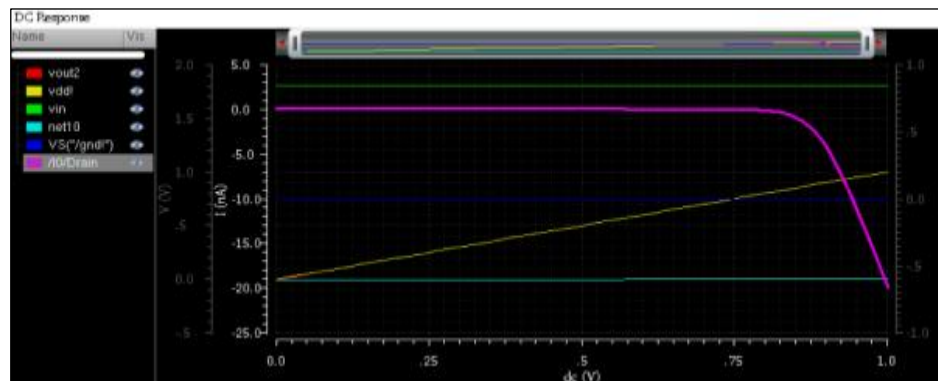


Figure 5h: Power analysis of full-adder using Hybrid GDI-CNTFET technology.
Source: Authors, (2026).

Simulation results indicated in Figure (5-c,d,e,f,g,h), demonstrate that the hybrid full adder achieves substantial reductions in average power consumption and propagation delay, resulting in a markedly improved power–delay product (PDP). These advantages make the proposed full adder design highly suitable for low-power arithmetic units and energy-constrained VLSI systems. The implementation of the XOR gate, 2×1 multiplexer and full adder using the proposed Hybrid GDI–CNTFET methodology clearly demonstrates its effectiveness. The results confirm that the hybrid approach successfully overcomes the voltage swing and noise margin limitations of CMOS-based GDI circuits while preserving their compact structure. At the same time, it mitigates the area overhead typically associated with CNTFET-only implementations. Similarly, for all the specified digital circuits, schematic has been implemented and verified, validated accordingly using Hybrid 32nm GDI-CNTFET based circuits in accordance with the 90nm CMOS technology, thereby the circuit parameters have been tabulated as shown in Table 1.

Table 1: Comparison of circuit parameters for CMOS and Hybri GDI-CNTFET technology.

Circuit	Technology	Node	Transist or Count	Average Delay (ps)	Average Power (μ w)	Power Delay Product (AJ)
NAND gate	CMOS	90nm	4	15	0.8	12
	Proposed Hybrid	32nm		2	0.1	0.2
OR gate	CMOS	90nm	6	12.5	2.8	35
	Proposed Hybrid	32nm		4.1	0.95	3.9
XOR gate	CMOS	90nm	8	20.5	6.5	133.25
	Proposed Hybrid	32nm		6.8	1.6	10.88
Half-Adder	CMOS	90nm	5	3.78	3.41	12.88
	Proposed Hybrid	32nm		0.98	0.75	0.74
Full-Adder	CMOS	90nm	8	30	1.5	45
	Proposed Hybrid	32nm		5	0.25	1.25
4-to-2 Encoder	CMOS	90nm	5	25	1.2	30
	Proposed Hybrid	32nm		4	0.2	0.8
2-to-4 Decoder	CMOS	90nm	20	45.8	18.5	847
	Proposed Hybrid	32nm		15.2	5.3	81
2x1 Multiplexer	CMOS	90nm	7	20	1	20
	Proposed Hybrid	32nm		3	0.15	0.45
D Flip-Flop	CMOS	90nm	5	3.78	3.41	12.88
	Proposed Hybrid	32nm		0.98	0.75	0.74
JK Flip-Flop	CMOS	90nm	16	25.5	15.6	397.8
	Proposed Hybrid	32nm		8.9	4.5	40.05

Source: Authors, (2026).

Overall, the proposed hybrid circuits achieve simultaneous optimization of power, delay, and area, validating the Hybrid GDI-CNTFET methodology as a promising design paradigm for next-generation low-power and high-performance VLSI systems.

V. SIMULATION RESULTS ANALYSIS AND DISCUSSION

The analysis for the simulation results observed for basic digital circuits, implemented using Hybrid GDI-CNTFET technology, were studied and represented in Figure 6.

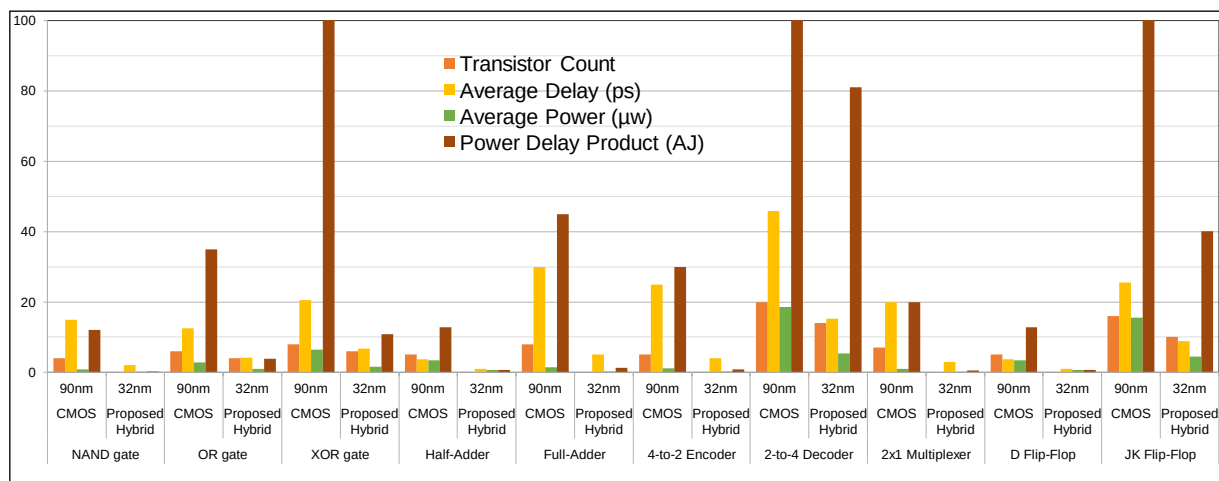


Figure 6: Analysis of CMOS and Hybrid GDI-CNTFET technology for various digital circuits.

Source: Authors, (2026).

The analysis presented details the Hybrid GDI-CNTFET circuits, designed using the 32nm GDI based CNTFET model in the Cadence Virtuoso environment, demonstrate significant performance advantages over traditional CMOS across a wide range of logic components, including NAND gate, OR gate, XOR gate, Half-adders, Full-adders, 4-to-2 Encoder, 2-to-4 Decoder, 2x1 Multiplexer, JK and D flip-flops by combining the low-transistor-count advantage of Gate Diffusion Input (GDI) logic with the high-speed, low-leakage properties of carbon nanotubes, the hybrid design achieves a vast reduction in power consumption and a notable decrease in transistor count.

The proposed hybrid GDI-CNTFET design methodology combines the structural efficiency of GDI with the higher electrical performance of CNTFETs. By using Stanford 32nm CNTFET model, which takes account of near-ballistic transport and threshold voltage dependent chirality, the design achieves full swing output transitions and eliminates the loss of threshold voltage, which occur in traditional GDI circuits based on CMOS technology. Simulations with different digital logic circuits (NAND, OR, XOR, half-adder, full-adder, multiplexer, encoder, decoder) and complex modules (D and JK flipflops) show 40-70 percent reduction in power and 45-70% increase in PDP compared to CMOS at 90nm. The hybrid approach also optimises the area by 25-55% than the standard CNTFET-based design, further reducing parasitic capacitance and allowing high speed operation. This design has a high noise margin and low leakage characteristics, which make it particularly suitable for low-power, high performance VLSI systems at the nanoscale. Future research can be by applying this methodology to sequential circuits such as clock registers, and then to complete systems-level designs like arithmetic logic units (ALUs) and memory structures. The validation of these designs by physical mapping and parasitic extraction will be a key step in the development of electronic technology.

VI. CONCLUSION AND FUTURE SCOPE

This research introduces a high performance design paradigm for the nanoscale regime, eliminating the dead zones and voltage degradation inherent in conventional GDI topologies and avoiding the classical trade-offs between logic density and signal integrity of CNTFETs. The comprehensive comparison shows that this Hybrid GDI-CNTFET framework leads to a significant reduction of the PDP and silicon area compared to conventional CMOS and the separate GDI-CNTFET implementations. This research has proven that it can withstand the short-circuit effects that are detrimental to traditional silicon based devices and thus provides a viable framework for scalable and energy-efficient next generation VLSI architectures. The results confirm that this approach is a key enabler for the next generation of small-scale, low-power digital signal processing and high-power computing systems. This methodology can be extended to more complex sequential circuits such as clocked registers where timing constraints are more significant and to design a full hybrid-based Arithmetic Logic Unit or explore memory structures such as SRAM. The proposed Hybrid GDI-CNTFET framework can be further extended to large-scale VLSI architectures to illustrate its scalability and system-level power-delay advantages, incorporating process-variation, thermal, and reliability analyses to illustrate the impact of CNT chirality dispersion, density non-uniformity, and device aging. Moving toward layout-level implementation and parasitic extraction will be necessary steps to further validate the industrial practicality of the hybrid GDI-CNTFET approach for future nano-electronic technologies.

VII. AUTHOR'S CONTRIBUTION

Conceptualization: Jayakrishna Padala, Kishore Kumar Kamarajugadda, Pavani Movva.

Methodology: Jayakrishna Padala, Kishore Kumar Kamarajugadda, Pavani Movva.

Investigation: Jayakrishna Padala, Kishore Kumar Kamarajugadda, Pavani Movva.

Discussion of results: Jayakrishna Padala, Kishore Kumar Kamarajugadda, Pavani Movva.

Writing – Original Draft: Jayakrishna Padala, Kishore Kumar Kamarajugadda, Pavani Movva.

Writing – Review and Editing: Jayakrishna Padala, Kishore Kumar Kamarajugadda, Pavani Movva.

Resources: Jayakrishna Padala, Kishore Kumar Kamarajugadda, Pavani Movva.

Supervision: Jayakrishna Padala, Kishore Kumar Kamarajugadda, Pavani Movva.

Approval of the final text: Jayakrishna Padala, Kishore Kumar Kamarajugadda, Pavani Movva.

VIII. ACKNOWLEDGEMENT:

I express my sincere gratitude to my Supervisor, Co-Supervisor, and Faculty of The ICAFI University, Raipur, for continuous guidance, encouragement, and support throughout the research work. I am deeply thankful for the facilities, technical assistance, and conducive research environment provided, which greatly contributed to the successful completion of the study.

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