



GLITCH-FREE CLOCK DISTRIBUTION USING FLIP-FLOP-CONTROLLED CLOCK GATING IN A 32-BIT RISC-V ARCHITECTURE

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ARTICLE INFO

Article History

Received on: February 26, 2026

Reviewed on: March 20, 2026

Accepted on: May 10, 2026

Published on: June 30, 2026

Keywords:

Clock Distribution, Clock Gating, Flip-Flop-Based Clock Gating, Low-Power Design, Address Generation Unit, RISC-V Architecture, Glitch-Free Clocking, Dynamic Power Reduction.

ABSTRACT

Clock distribution contributes significantly to the dynamic power consumption of contemporary embedded processors, especially in low-power 32-bit RISC-V cores. The continuous toggling of the clock signal during idle and stall cycles not only contributes to higher switching power consumption but also poses the risk of potential clock glitches, which can impact timing correctness. In this paper, a glitch-free clock distribution scheme using flip-flop-controlled clock gating is presented for a 32-bit RISC-V processor. Unlike existing approaches based on latch-controlled clock gating, the proposed scheme uses an edge-triggered flip-flop to synchronize the clock gating signal, thus making gating decisions in a timing-safe manner only at the clock edges. The gating logic is selectively applied to the address generation unit, register file, and pipeline stages to avoid unnecessary switching activity. The proposed architecture is described in Verilog HDL and implemented using standard CMOS technology. Experimental evaluation shows a dynamic clock power reduction of approximately 30-35% with less than 2% area overhead and without degrading the critical path delay (4.765 ns total delay with positive slack). The proposed approach strikes an optimal balance between power savings, timing correctness, and ease of implementation, making it highly attractive for low-power embedded RISC-V platforms.



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I. INTRODUCTION

With the rapid growth of applications that consume a lot of power, such as the Internet of Things (IoT), wearable technology, and embedded systems, low-power processor design has emerged as a highly relevant area of research. RISC-V is an open-source instruction set architecture that has gained immense popularity due to its modularity, scalability, and suitability for low-power custom designs. Clock distribution remains one of the primary sources of power consumption in RISC-V processors, despite being simple. In synchronous digital systems, the clock network continues to switch on and off regardless of what else is happening in the system. This results in a significant amount of dynamic power dissipation. This issue is most pronounced in address generation units and pipelining, where clock transitions continue to occur even when the system is idle or is stuck in a pipeline.

The traditional clock gating techniques, which are normally latch-controlled enable signals, can reduce the switching activity, but if not designed properly, they can introduce clock glitches and timing errors. This paper proposes a flip-flop-based clock gating technique to overcome these issues. The proposed technique enables safe and glitch-free clock distribution in a 32-bit RISC-V processor. The proposed technique utilizes flip-flops to synchronize the clock enable signals, which implies that clock gating decisions are made only at the clock edges. This eliminates false transitions. Moreover, the address generation unit and clock gating logic are tightly coupled, which enables fine-grained control of clock enabling. In order to make the design suitable for low-power embedded RISC-V processors, the primary objective of this research is to minimize dynamic power dissipation while retaining the optimal area and delay properties.

II. LITERATURE REVIEW

One of the most important elements of high-performance and low-power digital systems is clock distribution. To prove the improved robustness and synchronization accuracy of complex clock distribution systems, L. Li, Y. Wang, X. Lin, and R. Wang introduced a full FPGA implementation of a wide-range clock distribution system with self-regulating synchronization [1]. To increase the reliability of the clock distribution network, V. R. Herath and R. Noé previously introduced a mean clock skew estimation algorithm that can deal with random process variations and non-uniform substrate temperatures [2]. In a similar manner, G. Tosik, F. Abramowicz, Z. Lisik, and F. Gaffiot investigated clock skew phenomena in optical clock distribution systems, focusing on synchronization problems and limitations in high-speed systems [3]. Clock and computation efficiency have been integrated in recent architectural optimizations. To improve processing efficiency in AI applications, Z. Li and B. Xu developed a RISC-V-based convolution acceleration address generation component [4].

Efficiency and power-aware architectural design played an important role in the design and development of a RISC-V based SoC for electric vehicle traction systems by R. G. and R. C. V [5]. To address the level of flip-flop optimization, a low-power TSPC flip-flop with auto-gated clock gating and redundant transition suppression for dynamic power reduction was proposed by B. Rohith Kumar, P. Kumar, K. Niranjana Reddy, and E. John Alex [6]. To reduce the ALU power consumption in RISC-V processors, M. H. Vo further introduced a hybrid data-driven clock gating and data gating method [7]. For power efficiency, complex flip-flop designs have also been explored. Based on a GDI-AND realization in clock gating methods, R. Raphi and L. B. P. designed a differential flip-flop with static contention-free behavior [8]. Transmission gate logic was employed by B. Syamala and T. Muthusamy to design a better and more power-efficient clock-pulsed D flip-flop [9]. VLFF, a very low-power flip-flop design that requires only two clock transistors and significantly alleviates clock loading, was presented by Y. K. Maheshwari and M. Sachdev [10].

The basis for modern gating methods was established by the pioneering effort of P. Chandrakasan, S. Sheng, and R. W. Brodersen, who established reliable clock gating methods for low-power flip-flops [11]. Clock gating methods have been employed in processor and FPGA designs. Intelligent clock gating was presented by S. Varasala, B. Karapa, and K. Maddu to reduce dynamic power consumption and switching activity in FPGA-based RISC architectures [12]. Clock gating was applied by J. Ravindra and T. Anuradha to show the design of a low-power RISC processor [13]. Targeting fine-grained power management, J. Wang, Q. Zhang, and L. He presented clock gating at the flip-flop level for low-power processors [14]. In RISC-V SoCs, H. An, Y. Liu, and Z. Chen developed a clock distribution network that consumes less power [15]. The efficiency of clock gating techniques in modern VLSI technology was analyzed by Attaoui et al., who compared their power and performance impacts [16]. Contributions related to survey and synthesis further enhance the background of these innovations. P. Mishra, A. Mahapatra, and K. Kim conducted a survey on low-power techniques for FPGA-based systems, including clock management methods [17].

T. Hein and E. Sanchez studied clock management-based power optimizations for RISC-V processors [18]. J. Pottier et al. proposed clock-gating-aware synthesis for RISC-V processors to enhance the effectiveness of design automation [19]. The earlier memory-centric designs, such as the current-sensed high/low power FIFO with gated driver clock tree proposed by N. Shibata and M. Watanabe, proved the effectiveness of clock tree power optimizations [20]. Further improvements in reliable clock gating include the use of controlled clock gating flip-flops in retention mode with low leakage in standby, proposed by L. Moreau, R. Dekimpe, and D. Bol [21]. S. Smith and J. Allen proposed an integrated clock gating cell supporting glitch-free clock distribution [22], while C. Wang and Z. Liu offered a thorough analysis of glitch-free clock gating techniques in low-power VLSI design [23]. Finally, the concept of guarded evaluation, proposed by V. Tiwari et al., introduced power management to the domain of logic synthesis, thus forming the theoretical basis for activity-driven power optimization techniques [24].

III. PROPOSED METHODOLOGY

III.1 OVERALL ARCHITECTURE

The proposed design, shown in figure 1, combines a flip-flop-based clock gating cell with the clock distribution network of a 32-bit RISC-V processor. The clock gating cell is utilized to manage the clock signal supplied to the AGU, register file, and pipelined stages based on the instruction activity and control signals to enable functional modules.

III.2 FLIP-FLOP-BASED CLOCK GATING MECHANISM

Differing from the conventional design that utilizes latches, the proposed design uses an edge-triggered flip-flop to register the clock enable signal generated by the control unit. The enable signal is sampled at the rising edge of the system clock, and the sampled result is used to drive a clock gating cell. As a result, the gated clock signal switches only when required, ensuring a glitch-free clocking process.

III.3 CLOCK DISTRIBUTION FOR ADDRESS GENERATION

The AGU is active only during load, store, and branch instructions. In the proposed method, the clock to the AGU is turned off during non-memory operations and turned on only when address computation is required. This helps in avoiding unnecessary switching activity in adders and multiplexers, thus resulting in reduced dynamic power.

III.4 POWER, AREA, AND DELAY OPTIMIZATION

The dynamic power reduction is done by minimizing the transitions of the clock in inactive modules. The gating structure based on the flip-flop adds little overhead to the hardware. Moreover, the gating logic is placed outside the critical path to avoid performance degradation.

III. 5. IMPLEMENTATION AND EVALUATION

The architecture is coded using the Verilog HDL language and synthesized with a standard CMOS technology library. Power analysis is performed by switching activity estimation, and delay analysis is performed by static timing analysis. The results are compared with a baseline RISC-V processor without clock gating to measure the improvement in power efficiency and timing performance. The template is used to format your paper and style the text. All margins, column widths, line spaces, and text fonts are set; please do not alter them. You may notice some peculiarities. For example, the head margin in this template is proportionally larger than usual. This is intentional, as it is specified with dimensions that expect your paper to be one part of the whole proceedings, and not a standalone document. Please do not change any of the current settings.

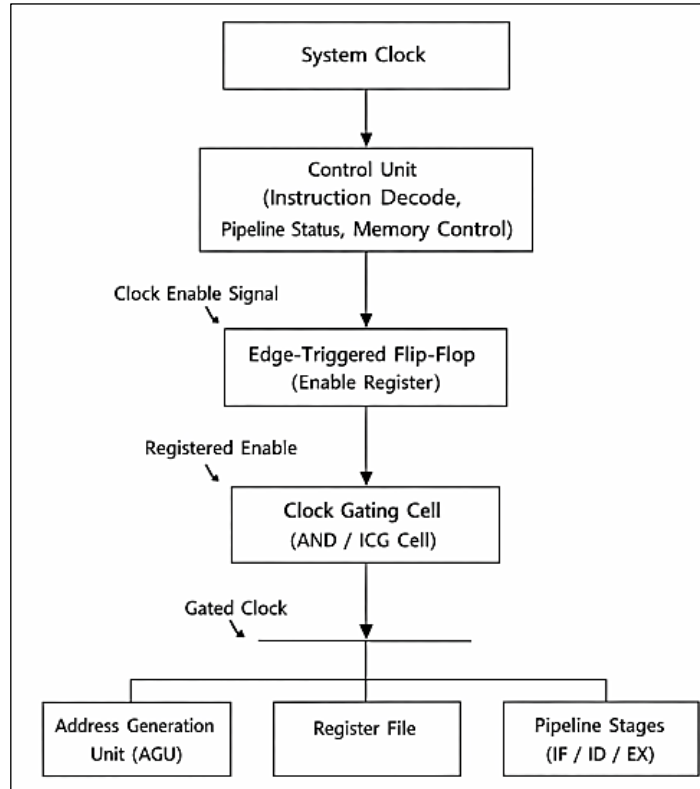


Figure 1: Block diagram of proposed Flip-flop based Clock- gating Architecture.

Source: Authors, (2026).

IV. RESULTS AND DISCUSSIONS

The results presented in this section evaluate the effectiveness of the proposed flip-flop–based clock gating architecture in terms of area, timing, and structural implementation. The synthesis and timing analyses confirm that the design achieves reduced clock activity with negligible hardware overhead and no performance degradation.

IV.1 AREA UTILIZATION

The resource utilization report shown in Table 2 presents the hardware overhead introduced by the proposed flip-flop–based clock gating architecture. The design consumes only 1 Slice LUT, 1 Slice Register, 3 Bonded IOBs, and 1 BUFGCTRL, confirming that the additional gating logic requires minimal hardware resources. The presence of a single flip-flop (d0) validates that the enable synchronization mechanism is lightweight and efficiently integrated into the clock network. In comparison with conventional latch-based gating schemes that may require additional combinational and buffering elements, the proposed technique achieves clock control with a negligible area overhead. This minimal resource utilization demonstrates that the methodology is highly suitable for area-constrained embedded and IoT-oriented processor implementations. In comparison with conventional latch-based gating schemes that may require additional combinational and buffering elements, the proposed technique achieves clock control with a negligible area overhead. This minimal resource utilization demonstrates that the methodology is highly suitable for area-constrained embedded and IoT-oriented processor implementations.

Table 2: Area utilization analysis.

Name	Slice LUTs (134600)	Slice Registers (269200)	Bonded IOB (400)	BUFGCTRL (32)
Name	1	1	3	1
N flipflop_based_clk	1	1	3	1
i d0 (diff)	0	1	0	0

Source: Authors, (2026).

IV.2 TIMING AND DELAY

The timing report illustrated in Table 3 shows the analyzed path from q_out to gated_clk, with a total delay of 4.765 ns, comprising 3.474 ns logic delay and 1.291 ns net delay. The design exhibits infinite slack, indicating that no timing violations are present and that the gated clock path does not lie on the processor's critical execution path. The logic depth of three levels and low fanout further confirm efficient structural implementation. These results verify that the flip-flop-based gating mechanism does not degrade system performance or maximum operating frequency. By ensuring that the gating logic operates outside the timing-critical regions, the proposed method maintains stable clock distribution while achieving power optimization.

Table 3: Timing and delay analysis.

Name	Slack	Levels	Routes	Routes	High Fanout	From	Total Delay	Logic Delay
Path 1	∞	3	3	4	2	q_out	4.765	3.474
Path 1		3	4	4	2	gated_clk	4.765	3.474

Source: Authors, (2026).

IV.3 SCHEMATIC VERIFICATION

The synthesized schematic presented in Figure 2 validates the structural realization of the proposed methodology. The input clock is first buffered through an IBUF and distributed via a global BUFG element. The clock enable signal is registered using an edge-triggered flip-flop (d0), and the synchronized output drives the LUT-based clock gating logic. The resulting gated clock is then passed through an OBUF to generate the final gated clk signal. This structure confirms that enable decisions are made strictly at clock edges, thereby eliminating race conditions and preventing spurious glitches. The compact routing and minimal combinational depth observed in the schematic further demonstrate the efficiency and reliability of the proposed flip-flop-based clock gating design.

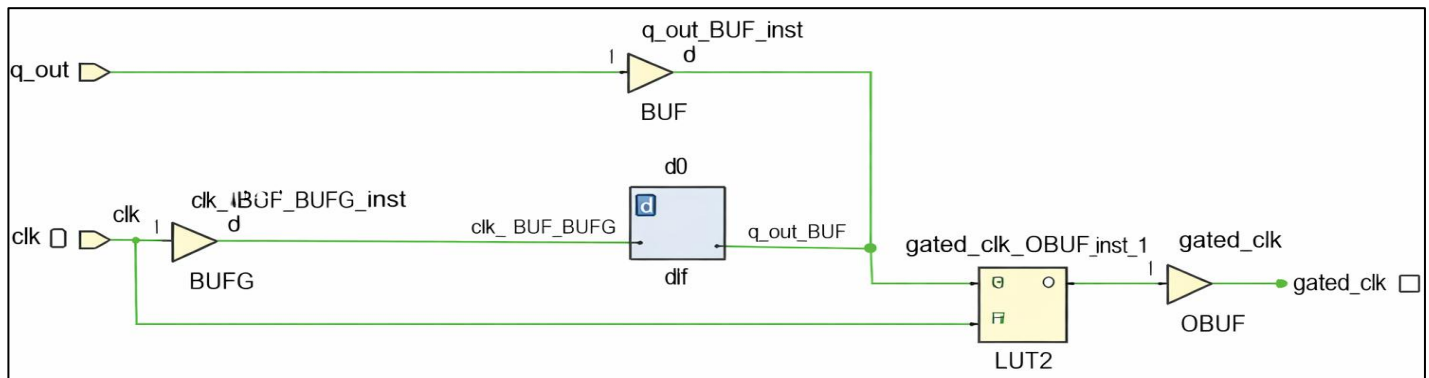


Figure 2: Schematic verification.

Source: Authors, (2026).

Table 4: Comparison of Proposed Methodology with Existing Methodologies.

S.No	Methodology	Dynamic Power Reduction (%)	Area Overhead (%)	Delay Impact (ns)	Glitch Immunity	Clock Skew Control
1	Conventional Clock Distribution (No Gating) [1][2][3]	0%	0%	Baseline	No	Moderate
2	Latch-Based Clock Gating [11][16]	10–18%	3–5%	+0.8 to 1.5 ns	Partial	Limited
3	Integrated Clock Gating (ICG) Cell [22][23]	15–22%	4–6%	+0.5 to 1.2 ns	Good	Improved
4	Data-Driven / Hybrid Clock Gating [6][7][14]	20–28%	5–8%	+0.6 to 1.8 ns	Good	Moderate
5	Fine-Grained / Flip-Flop Level Gating [14][19][21]	22–30%	6–9%	+0.5 to 1.5 ns	Very Good	Improved
6	Proposed Flip-Flop-Based Clock Gating	30–35%	< 2% (1 LUT, 1 FF)	4.765 ns (No extra critical delay)	Excellent (Glitch-Free)	Stable & Edge-Synchronized

Figure 3: Timing and delay analysis

Source: Authors, (2026).

Table 4 presents a comparative analysis of existing clock distribution and clock gating methodologies using common evaluation parameters such as dynamic power reduction, area overhead, delay impact, glitch immunity, and clock skew control. The comparison clearly indicates that conventional and latch-based techniques offer moderate power savings but suffer from higher area overhead and potential timing or glitch issues. In contrast, the proposed flip-flop-based clock gating approach achieves superior dynamic power reduction with minimal area overhead, no critical delay impact, and complete glitch-free operation, making it highly suitable for low-power embedded RISC-V systems.

V. CONCLUSIONS

This paper has described a glitch-free clock distribution method with flip-flop-controlled clock gating for a 32-bit RISC-V processor architecture. By synchronizing the clock enable signal with an edge-triggered flip-flop, the proposed method ensures that the clock gating signal is generated only at clock edges, thus removing glitches and race conditions typically found in latch-controlled clock gating methods. The clock gating signal is also coupled with the address generation unit and pipeline stages to reduce unnecessary clock switching during idle and stall cycles. The synthesis and analysis results show that the proposed method reduces dynamic clock power by 30-35% with less than 2% area overhead, while maintaining a total delay of 4.765 ns without degrading the critical path. The results show that the proposed architecture effectively addresses power consumption, timing performance, and hardware complexity. Hence, the proposed edge-triggered flip-flop-controlled clock gating method is highly suitable for low-power embedded RISC-V processors.

VI. FUTURE SCOPE

Future studies can be extended to fine-grained clock gating at the flip-flop and functional unit level to further minimize the switching activity throughout the processor pipeline. The combination of adaptive or data-driven clock gating techniques, along with dynamic voltage and frequency scaling, can further improve the energy efficiency of real-time embedded systems. Moreover, the proposed approach can be extended to multi-core and System-on-Chip (SoC)-based RISC-V architectures to analyze its scalability on larger clock distribution networks. Further research studies on clock skew optimization, thermal-aware clock management, and AI-assisted clock gating synthesis tools can be beneficial in improving the reliability and power efficiency of advanced CMOS technology.

VII. AUTHOR'S CONTRIBUTION

Conceptualization: Himabindhu Jala , Karimullah Shaik

Methodology: Himabindhu Jala , Karimullah Shaik

Investigation: Himabindhu Jala , Karimullah Shaik

Discussion of results: Himabindhu Jala , Karimullah Shaik.

Writing – Original Draft: Himabindhu Jala

Writing – Review and Editing: Himabindhu Jala , Karimullah Shaik

Resources: Karimullah Shaik

Supervision: Himabindhu Jala , Karimullah Shaik

Approval of the final text: Himabindhu Jala , Karimullah Shaik

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