



RESEARCH ARTICLE

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IMPLEMENTATION AND SIMULATION OF SWITCH CAPACITOR PASSIVE RC INTEGRATOR IN DEEP SUB MICRON TECHNOLOGY

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ABSTRACT

Switches and capacitors are utilized in place of a resistor R in the switched-capacitor circuit, with a MOSFET serving as the switch. In this paper, the standard RC integrator is compared with the switch capacitor RC integrator. The design is simulated first, and solutions to the design issues are explored and implemented in 180nm technology. The analysis demonstrates that NMOS transistor performance strongly depends on the W/L ratio. As resistance decreases sharply with increasing W/L , current delivery efficiency enhances. Drain current increases substantially with larger widths due to improved channel conduction. This study analyzes the electrical behavior of an NMOS transistor for varying device widths while keeping the channel length constant. The investigation focuses on the effect of the width-to-length (W/L) ratio on drain current (I_D), on-resistance (R_{on}), and related process parameters. The results demonstrate a strong dependence of I_D and R_{on} on device geometry, consistent with MOSFET theory.



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I. INTRODUCTION

RC Integrator can be used as low-pass filter in many applications. In devices like variable speed wipers and pacemakers, it can also serve as a timer [1]. Large-value resistors, which take up a lot of chip space, are required for typical RC circuits. Switches and capacitors are used in place of resistors in Switched-Capacitor (SC) circuits, which can assist in minimizing the chip area. It uses two switches to control the flow of charges into and out of a capacitor. The capacitance ratio determines the characteristics of a switched capacitor circuit. One capacitor C and two switches S_1 and S_2 take the place of the resistor R in switched capacitor integrator circuits (SCI). This is shown in Figure 1 [2], [3].

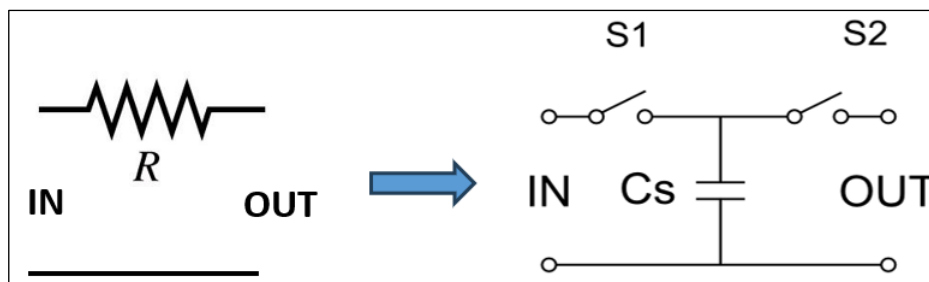


Figure 1: Resistor as a Switched-Capacitor.
Source: Authors, (2026).

The value of the capacitor C_s and the switching frequency f determine the value of resistance R .

$$R = \frac{V}{I} = \frac{1}{C_s f} \quad (1)$$

In this work, the switch is implemented using MOSFET transistors, as shown in Figure 2. They provide fast, low-power, accurate, and easily integrable switching, which is essential for precise charge transfer. When a MOSFET is used as a switch, it has some nonidealities, which are discussed in the next section [4], [5].

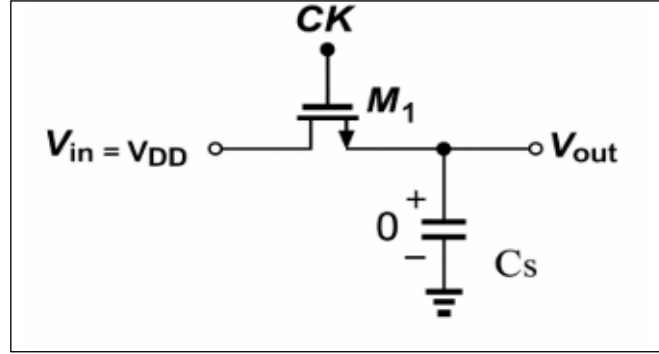


Figure 2: Switched Capacitor Resistor.
Source: Authors, (2026).

II. NONIDEALITIES OF MOSFET SWITCH

Three sorts of nonideal effects can occur when a MOSFET is employed as a switch: (i) Non-Linear R_{on} (ii) Charge Injection and (iii) Clock Feed Through [6-8].

II.1 NON-LINEAR R_{on} (Between Drain and Source)

The $nMOS$ is ON by applying a positive gate signal equal to V_{DD} . When the value of $V_{GS} - V_{thn}$ become grater then V_{DS} , the $nMOS$ is operating in the triode region. The current I_D is given by equation 2 [9].

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{in} - V_{thn}) V_{DS} \quad (2)$$

The equivalent resistance R_{on} is found by dividing V_{DS} by with I_D (here body effect has ignored.)

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{in} - V_{thn})} \quad (3)$$

The R_{on} depends on the input signal V_{in} , therefore, its value changes with V_{in} . The R_{on} The size of an nMOS transistor is small because the $\mu_n C_{ox}$ is large. The PMOS transistor is large because the $\mu_p C_{ox}$ is small. Consequently, a low value of R_{on} makes the pMOS transistor less appropriate. Compared to both nMOS and pMOS, the CMOS transmission gate (TG) has a higher value of R_{on} . The values of R_{on} for nMOS, pMOS, and TG are displayed in Figure 3.

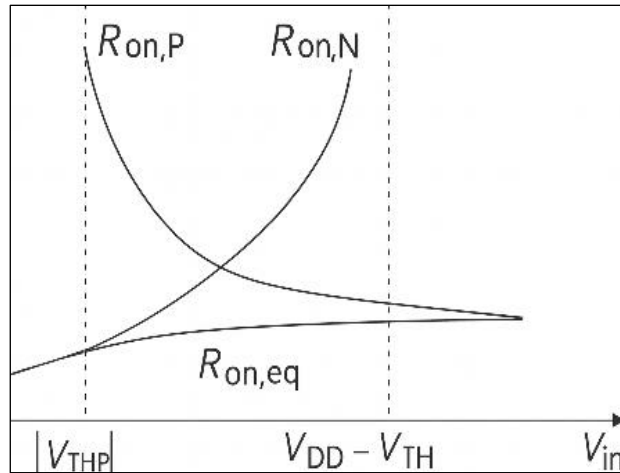


Figure 3: R_{on} for pMOS, nMOS, and TG.
Source: Authors, (2026).

II.2 CHARGE INJECTION

A channel is created between the source and drain when nMOS is turned on. Equations 4 [10], [11] provide the charge Q_{ch} stored in the channel.

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{thn}) \quad (4)$$

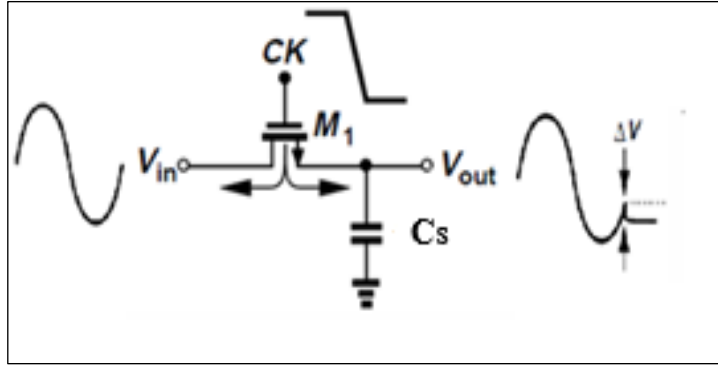


Figure 4: Charge Injection Effect on MOS Switch.

Source: Authors, (2026).

When the nMOS turned off, the charge present in the channel is distributed between the capacitor and the input, as shown in Figure 4 [12]. The clock turnoff slope, the input-to-output capacitance ratio, and the drain-source voltage factors all affect this charge. This charge does not affect the input side, but it changes the voltage stored on the output capacitor C_s as shown in equation 5.

$$\Delta V = Q_{ch}/2C = WLC_{ox}(V_{DD} - V_{in} - V_{thn})/2C \quad (5)$$

II.3 CLOCK FEED THROUGH

The parasitic capacitance between the MOSFET's terminals must be depicted as indicated in Figure 5 to comprehend the clock feed-through effect. In this case, the nMOS is operating in the Triode region and is regarded as being ON. The clock signal passes via the gate-source and gate-drain capacitances as the gate clock signal rises [13], [14].

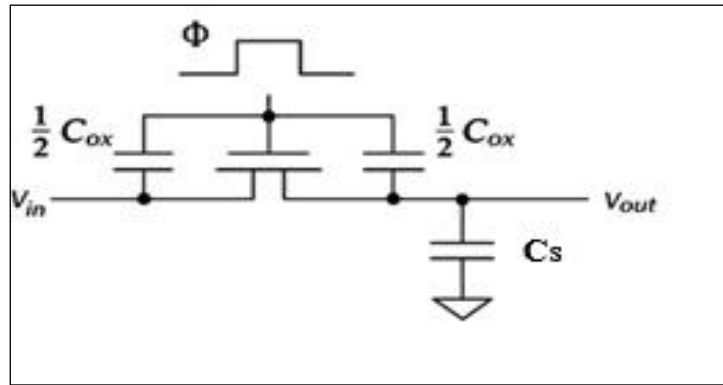


Figure 5: Clock feed through Effect on MOS Switch.

Source: Authors, (2026).

The input signal V_{in} is available at the output capacitor when the nMOS is turned on by applying V_{DD} at the gate terminal. In this instance, V_{out} is unaffected by the capacitive feed-through and the capacitor C_s charged to V_{in} . The nMOS switches off when the clock signal changes to low. In this instance, the capacitance C_s and the gate-drain/source capacitance are separated by a (capacitive) voltage divider. As a result, equation 6 provides the value of a clock signal port that is present across C_s .

$$\Delta V_{load} = \frac{C_{overlap}(V_{DD} - V_{ss})}{C_{overlap} + C_{load}} \quad (6)$$

Where $C_{overlap}$ is the overlap capacitance, and its value is given by equation 7.

$$C_{overlap} = C_{ox}WLD \quad (7)$$

The gate length that overlaps the drain and source is represented by the symbol, LD in Equation (7).

III. SOLUTION OF MOSFET NONIDEALITIES

The following techniques can reduce the nMOS Switch's nonidealities [15], [16].

III.1 NON-LINEAR R_{on} (Between Drain and Source)

The value of R_{on} can be reduced by increasing the W/L ratio or reducing V_{in} and V_{thn} . The R_{on} remains almost constant for the transmission gate if the switch is replaced by a transmission gate.

III.2 CHARGE INJECTION

As illustrated in Figure 6, connect a dummy switch in series with a nMOS switch. The dummy switch can be made to be half the size of the primary switch. Both the source and the drain are connected. When the nMOS switch is off, the dummy switch compensates for the charge by allowing the 50% channel charge to flow toward the capacitor (C_s) [17].

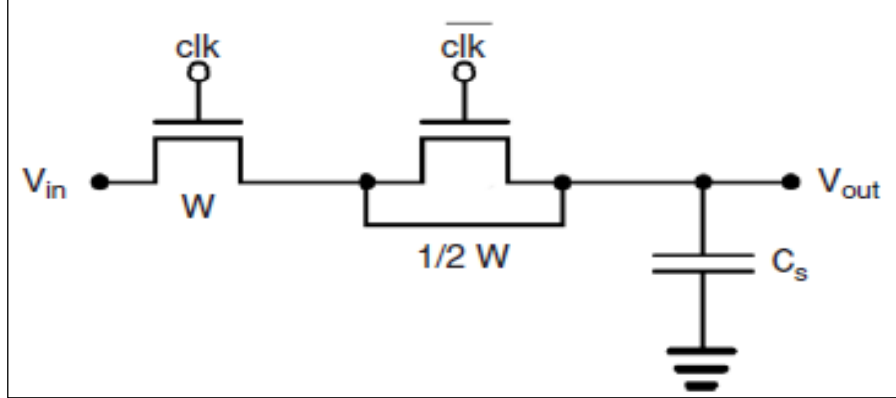


Figure 6: Use of a dummy switch to remove Charge Injection.
Source: Authors, (2026).

III.3 CLOCK FEED THROUGH

Here, the dummy switch suppresses the effect of clock feed through, as shown in Figure 7. A dummy transistor M_2 removes the charge introduced by the primary transistor. After M_1 shuts off and M_2 turns on, the channel charge deposited by M_1 on C_s is absorbed by M_2 to form a channel because the M_2 is driven by $\overline{CK}$. The charge injected by M_1 , Δq_1 is equivalent to the charge absorbed by M_2 if $W_2 = 0.5W_1$.

$$\Delta q_1 = \frac{W_1 L_1 C_{ox}}{2} (V_{CK} - V_{in} - V_{THN})$$

$$\Delta q_2 = W_2 L_2 C_{ox} (V_{CK} - V_{in} - V_{THN})$$

If $W_2 = 0.5W_1$ and $L_2 = L_1$, the effect of clock feedthrough is suppressed. The whole charge in V_{out} is going to be zero as per equation (8).

$$-V_{CK} \frac{W_1 C_{ov}}{W_1 C_{ov} + C_s + 2W_2 C_{ov}} + V_{CK} \frac{2W_2 C_{ov}}{W_1 C_{ov} + C_s + 2W_2 C_{ov}} = 0 \quad (8)$$

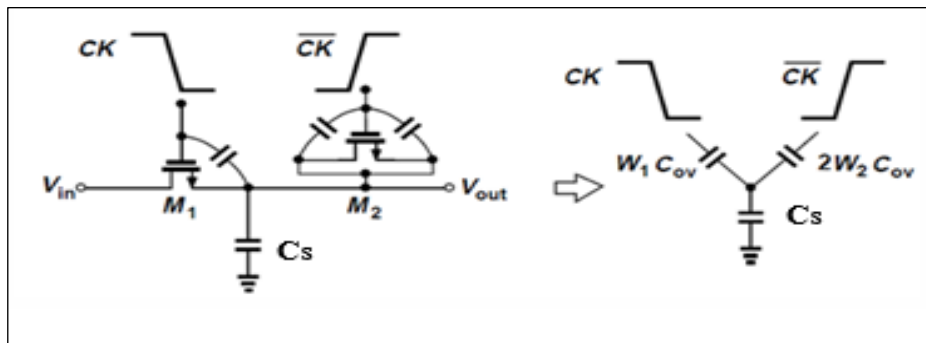


Figure 7: Use of the TG switch to remove Clock Feed Through.
Source: Authors, (2026).

IV. RESULTS AND DISCUSSION

This study analyzes the electrical behavior of an NMOS transistor for varying device widths while keeping the channel length constant. The investigation focuses on the effect of the width-to-length (W/L), ratio on drain current (I_D), on-resistance (R_{on}), and related process parameters. The results demonstrate a strong dependence of I_D and R_{on} on device geometry, consistent with MOSFET theory. MOSFETs exhibit electrical characteristics highly dependent on device geometry. In this work, NMOS properties are evaluated for various widths while keeping the channel length constant ($L = 0.18 \mu\text{m}$). The study investigates the effects of W/L scaling on on-resistance (R_{on}) and drain current (I_D) [18]. Modern semiconductor design relies on MOSFET scaling, which has a direct impact on power consumption, device performance, and switching speed. A key component of both digital and analog circuits, the NMOS transistor has properties that are strongly influenced by its physical shape. The W/L ratio is one of these characteristics that significantly influences channel conduction capabilities. This work assesses the electrical properties of NMOS for various widths between $2 \mu\text{m}$ and $100 \mu\text{m}$. A fixed channel length of $0.18 \mu\text{m}$ is shared by all devices [19]. Quantifying the effects of W/L scaling on drain current (I_D), on-resistance (R_{on}), and overall conduction behaviour is the goal. To verify MOSFET operation under strong inversion, these practical findings are contrasted with theoretical predictions [3].

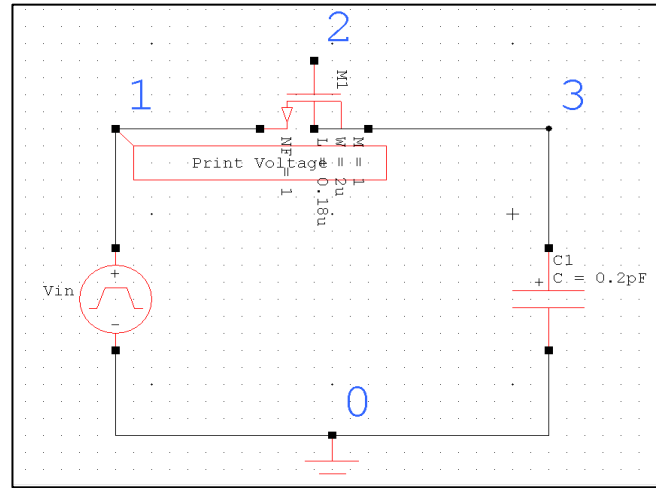


Figure 8: nMOS Switch with Pulse input.
Source: Authors, (2026).

IV.1 NON-LINEAR R_{on} (Between Drain and Source)

To guarantee that differences in electrical behaviour are solely due to geometric scaling, the devices under analysis have the same material and manufacturing parameters. The following is a list of the important parameters:

- Channel length (L): $0.18 \mu\text{m}$
- Device widths (W): $2, 10, 20, 50$, and $100 \mu\text{m}$
- Electron mobility (μ_n): $1400 \text{ cm}^2/\text{V}\cdot\text{s}$
- Oxide capacitance (C_{ox}): $8.65 \times 10^{-8} \text{ F}/\text{cm}^2$
- Oxide thickness (t_{ox}): 4.1 nm
- Oxide permittivity (ϵ_{ox}): $3.51 \times 10^{-13} \text{ F}/\text{cm}$
- Vacuum permittivity (ϵ_0): $8.85 \times 10^{-14} \text{ F}/\text{cm}$
- Gate voltage (V_{GS}): 1.8 V
- Threshold voltage (V_{thn}): 0.3725327 V

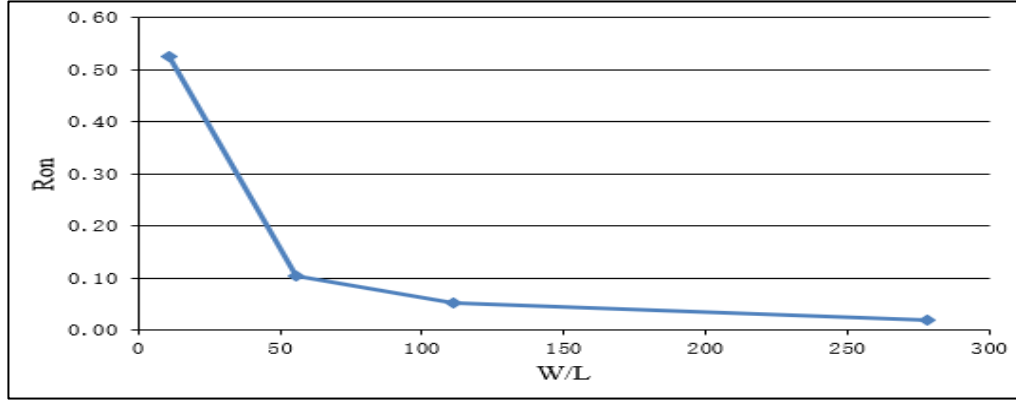
The effective gate overdrive voltage $V_{GS} - V_{thn}$ remains constant at 1.427 V , ensuring consistency in theoretical calculations such as R_{on} and I_D .

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{in} - V_{thn})} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{thn})} \quad (9)$$

Table 1: Parameters for variation in R_{on} with respect to W/L .

Sr.No.	$W \text{ } \mu\text{m}$	$W/L \text{ } \mu\text{m}$	V_{GS}	V_{thn}	$V_{GS} - V_{thn}$
1.	2	11.11	1.8 V	0.3725327	1.427 V
2.	10	55.56	1.8 V	0.3725327	1.427 V
3.	20	111.11	1.8 V	0.3725327	1.427 V
4.	50	277.78	1.8 V	0.3725327	1.427 V
5.	100	555.56	1.8 V	0.3725327	1.427 V

Source: Authors, (2026).

Figure 9: Variation in R_{on} with respect to W/L .

Source: Authors, (2026).

Table 1 illustrates how R_{on} dropped from $0.525 \text{ } \Omega$ to $0.0105 \text{ } \Omega$ over the same range. The inverse reliance on W/L is consistent with theory.

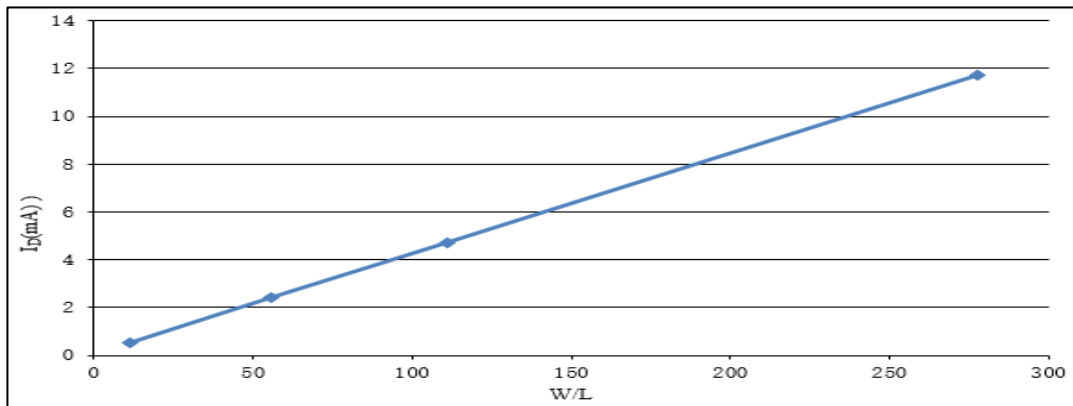
IV.1.1 Drain Current $I_D(\text{mA})$

By changing the device width while maintaining a constant channel length, this study examines the electrical behaviour of an NMOS transistor. As indicated in Table 2, the analysis focuses on how the width-to-length (W/L) ratio affects the drain current (I_D). In line with MOSFET theory, the results demonstrate a significant influence of I_D on device geometry.

Table 2: Parameters for variation in $I_D(\text{mA})$ with respect to W/L .

Sr.No.	$W \text{ } \mu\text{m}$	$W/L \text{ } \mu\text{m}$	$I_D(\text{mA})$
1.	2	11.11	0.5
2.	10	55.56	2.4
3.	20	111.11	4.72
4.	50	277.78	11.74

Source: Authors, (2026).

Figure 10: Variation in I_D due to W/L .

Source: Authors, (2026).

Drain current increased from 0.50 mA ($W/L = 11.11$) to 11.74 mA ($W/L = 277.78$). This shows proportional scaling with width, which is consistent with strong inversion MOSFET equations.

IV.2 CHARGE INJECTION

Charge injection in MOSFET switches occurs when charge stored in the channel is released into the drain and source nodes during the turn-off transition. The channel charge and the amount of injected charge are directly correlated, which increases with device width and hence with a higher W/L ratio. Table 3 shows that as the W/L ratio increases, more charge is transferred to the connected node, resulting in a larger voltage disturbance across the load capacitance. This explains the observed increase in voltage drop (charge injection effect) with increasing W/L ratio in figure 11.

Table 3: Parameters for voltage drop (mV) with respect to W/L .

Sr.No.	W μm	W/L μm	Voltage drop (mv)
1.	2	11.11	0.06
2.	10	55.56	0.28
3.	20	111.11	0.51
4.	50	277.78	1.02

Source: Authors, (2026).

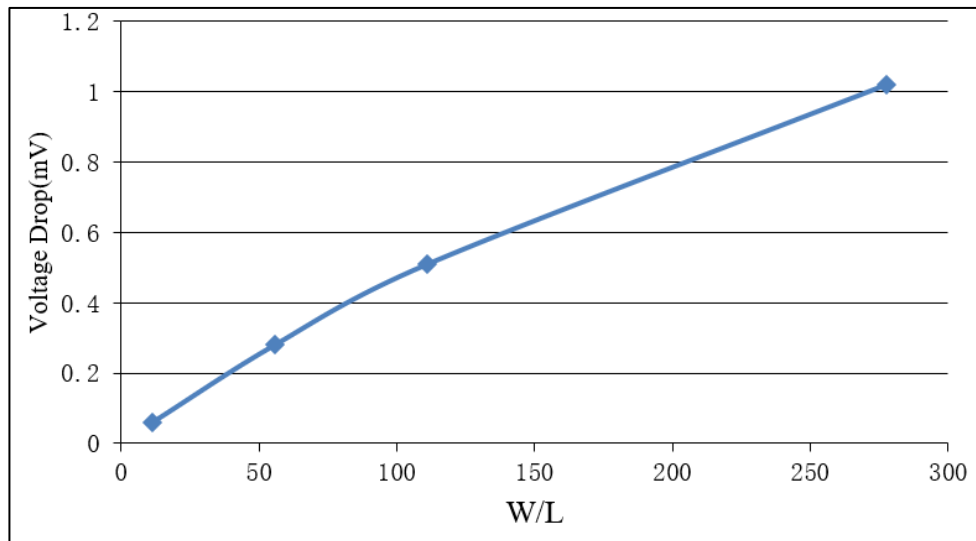


Figure 11: Effect of Charge Injection with respect to W/L .

Source: Authors, (2026).

Figure 11 displays the relationship between the Voltage Drop (in millivolts, mV) and the W/L ratio, which typically represents the width-to-length ratio of a MOSFET, in integrated circuits or electronic design. As the W/L ratio increases, the voltage drop across the component also increases proportionally. Figure 11 illustrates how increasing W/L increases the effect of charge injection from 0.1 to 1.1. In Figure 8, when the width is scaled down from 50 μm to 2 μm , the simulation results in Figures 12 and 13 show a significant reduction in charge injection due to the decreased channel charge associated with smaller device dimensions.

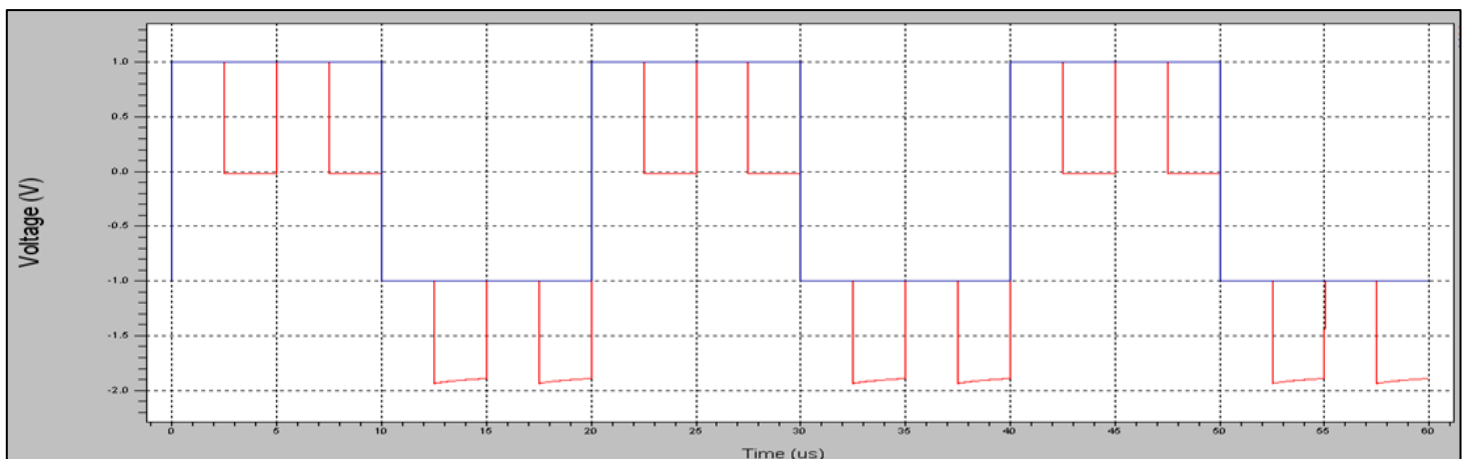


Figure 12: Effect of Charge Injection on W/L for $W=50$ μm .

Source: Authors, (2026).

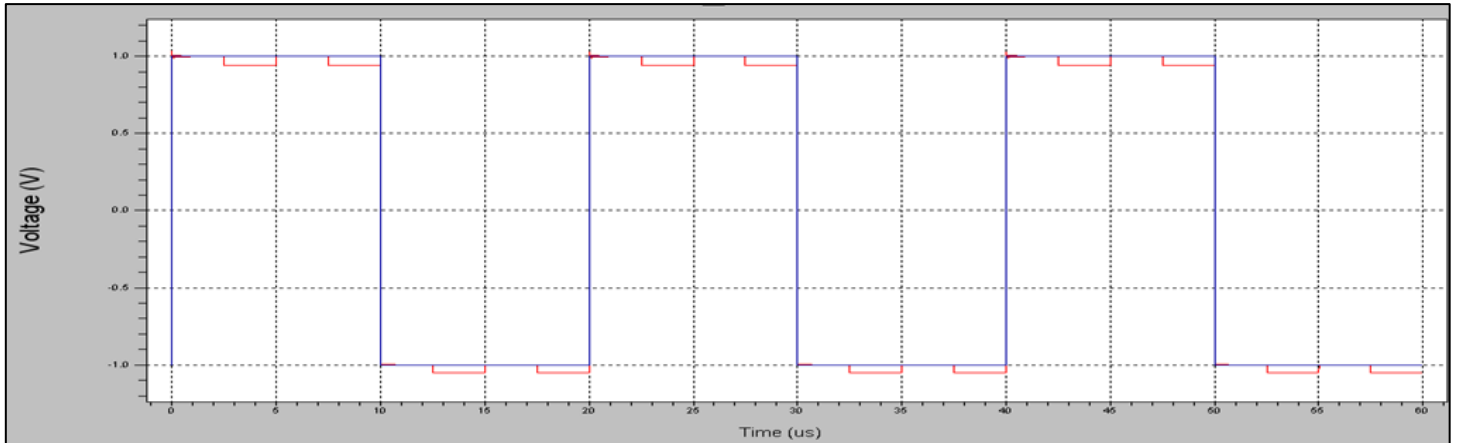


Figure 13: Effect of Charge Injection on W/L for $W=2\ \mu\text{m}$.
Source: Authors, (2026).

IV.3 CLOCK FEED THROUGH

In Figure 8, a dummy switch transistor is added in series with the main switching transistor, as shown in Figure 14. When we simulate Figure 14, it will effectively minimize both charge injection and clock feedthrough effects, as shown in Figure 15. The dummy transistor compensates for the injected charge during switching, resulting in improved accuracy and performance of the circuit. Overall, the combined approach of transistor width reduction and dummy switch implementation proves to be an effective technique for mitigating charge injection effects in switched-capacitor circuits.

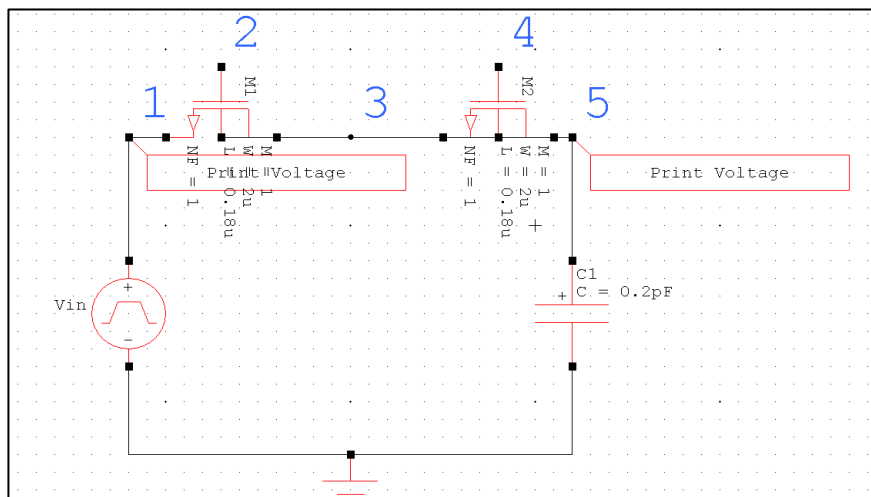


Figure 14: Reduction of clock feed-through using a dummy transistor.
Source: Authors, (2026).

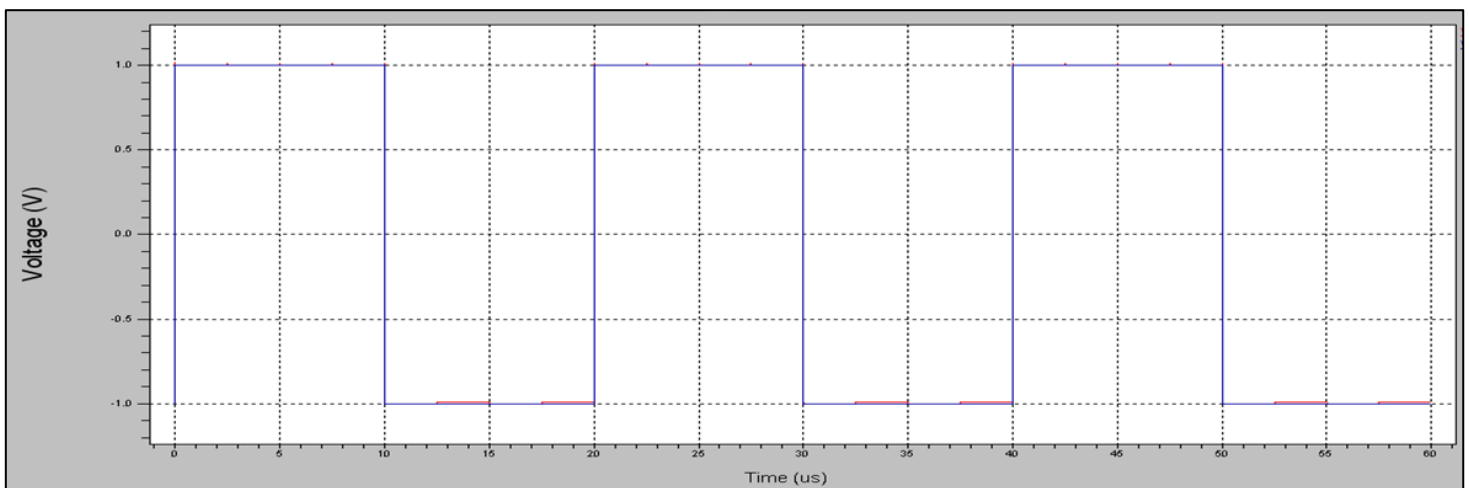


Figure 15: Clock feed through and Charge Injection reduction by dummy transistor.
Source: Authors, (2026).

V. CONCLUSION

The application of MOSFET switches in SC circuits is examined. The MOSEFT switch's shortcomings are described. Implementation and simulation results are presented for the solutions of the MOSEFT switch non-idealities. Increasing W/L improves NMOS performance by increasing I_D and reducing R_{on} . Process parameters were constant, confirming that geometry was the primary factor influencing electrical behavior. These results support further research into NMOS scaling and performance modeling. The analysis reveals that the W/L ratio significantly affects NMOS transistor performance. Important conclusions include:

1. Because of better channel conduction, the drain current rises significantly with wider channels.
2. As W/L increases, on-on resistance drastically drops, improving current delivery efficiency.
3. Process parameters that are consistent guarantee that changes are only the result of geometric scaling.
4. Device validity is confirmed by measured results that match theoretical MOSFET models.

These results contribute to MOSFET scaling and performance modelling research and encourage additional device optimisation studies.

VI. AUTHOR'S CONTRIBUTION

Conceptualization: Mehulkumar Patel, Kehul Shah, Haresh Judal, Devendra Patel and Roshni Chaudhari.

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Investigation: Mehulkumar Patel, Kehul Shah, Haresh Judal, Devendra Patel and Roshni Chaudhari.

Discussion of results: Mehulkumar Patel, Kehul Shah, Haresh Judal, Devendra Patel and Roshni Chaudhari.

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Writing – Review and Editing: Mehulkumar Patel, Kehul Shah, Haresh Judal, Devendra Patel and Roshni Chaudhari.

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Approval of the final text: Mehulkumar Patel, Kehul Shah, Haresh Judal, Devendra Patel and Roshni Chaudhari.

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